Addendum for Operation Manuals
SPI Protocol
Matrix SPI Displays

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1 Message frame

Table 1. SPI message frame

SOF	Command	[Address]/Data	Check	EOF
"1111 1111" (FF_h)	8 bits	N x 8 bits	XOR	"0101 0101" (55_h)

SOF (Start of Frame) is the only byte in frame where most significant bit (MSB) is '1'. All other bytes in frame have MSB set to '0'.

2 Row number

Some commands require defining a row number. Row address is 14 bits long carried inside a 16-bit word.

Table 2. Row number to address table

Row number	Address															
	0	B13	B12	B11	B10	B9	B8	B7	**0**	B6	B5	B4	B3	B2	B1	B0	**(hex)**
1	**0**	0	0	0	0	0	0	0	**0**	0	0	0	0	0	0	1	00_h 01_h
2	**0**	0	0	0	0	0	0	0	**0**	0	0	0	0	0	1	0	00_h 02_h
3	**0**	0	0	0	0	0	0	0	**0**	0	0	0	0	0	1	1	00_h 03_h
…																	…
127	**0**	0	0	0	0	0	0	0	**0**	1	1	1	1	1	1	1	00_h $7F_h$
128	**0**	0	0	0	0	0	0	1	**0**	0	0	0	0	0	0	0	01_h 00_h
129	**0**	0	0	0	0	0	0	1	**0**	0	0	0	0	0	0	1	01_h 01_h
…																	…
238	**0**	0	0	0	0	0	0	1	**0**	1	1	0	1	1	1	0	01_h $6E_h$
239	**0**	0	0	0	0	0	0	1	**0**	1	1	0	1	1	1	1	01_h $6F_h$
240	**0**	0	0	0	0	0	0	1	**0**	1	1	1	0	0	0	0	01_h 70_h

3 SPI protocol

3.1 Commands

Command	**Hex #**	**Binary**							
Write complete display data	01_h	0	0	0	0	0	0	0	1
Write display block (multiple rows)	02_h	0	0	0	0	0	0	1	0
Write one row	04_h	0	0	0	0	0	1	0	0
Clear screen (full black or full transparent)	19_h	0	0	0	1	1	0	0	1
All pixels ON (full yellow)	$1A_h$	0	0	0	1	1	0	1	0
Invert display image	$1C_h$	0	0	0	1	1	1	0	0
Write frame frequency	61_h	0	1	1	0	0	0	0	1
Communication period	62_h	0	1	1	0	0	0	1	0

3.1.1 Write complete display data

Pixels are going from left to right from top to bottom. A first pixel in a byte is the most significant one. See Figure 1 for reference.

Command	**Data1 … DataN**			**Check**
01_h	**Data1** 8bits	**----** 8bits	**DataM** See Equation 1	
	DataM+1 8bits	**----** 8bits	**Data** See Equation 1	
	- -	- -	- -	
	Data 8bits	**----** 8bits	**DataN** See Equation 1	Xor(Command,Data)

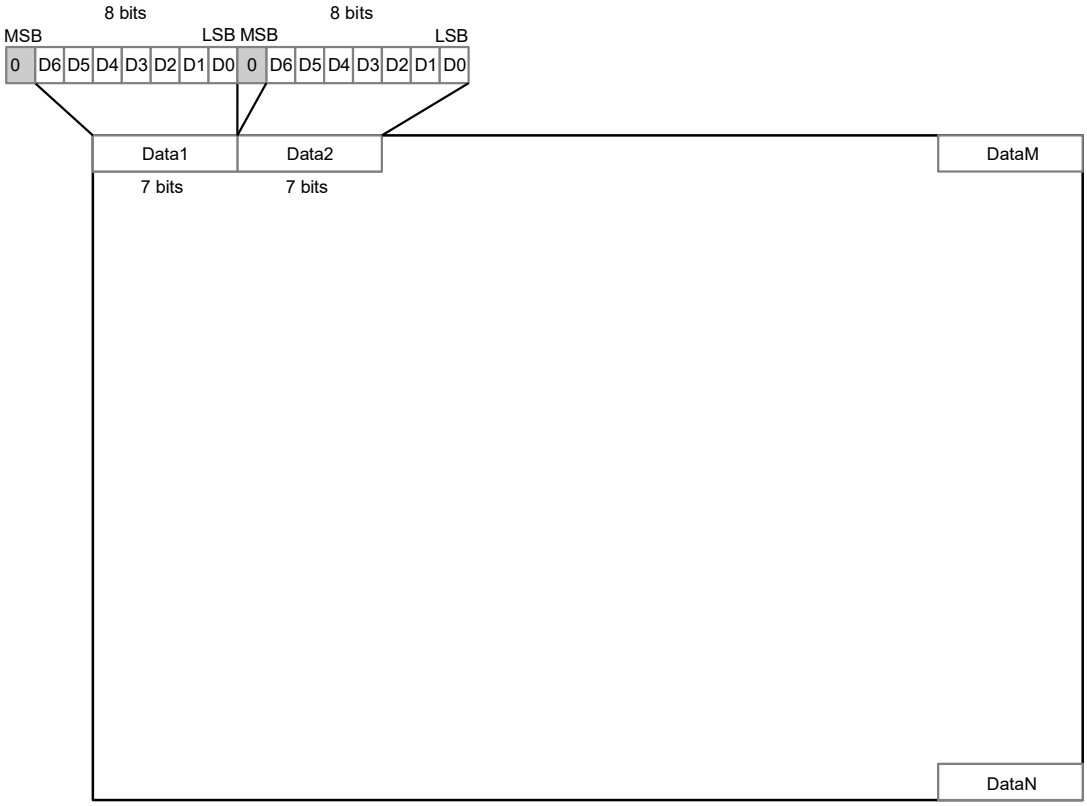

Figure 1. Display pixel locations on image data mapping.

Each row of data should be 8 bits divisible. If the last byte of row does not fill up with the display data, the last byte of the row must be complemented with a required number of bits set to '0'. The number of '0' bits to be added at the end of the last row byte (DataM) can be calculated using the following equation.

7 – (columns - (INT (columns / 7) * 7)).

Equation 1. Row last byte '0' fill up calculation

E.g. EL320.240 display have 320 column pixels each row. According to Equation 1 the number of appending bits set to '0' will be 2 [7-(320 -INT (320/7) *7)) = 2].

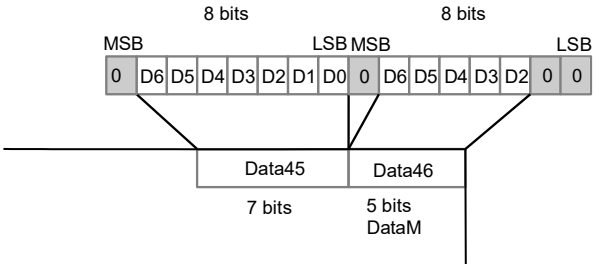

Figure 2. An example of generating the last byte of row on EL320.240 display.

3.1.2 Write display block (multiple rows)

Command	First row address	Last row address	First bits first row	----	Last bits of last row	Check
02_h	16 bits See Table 2	16 bits See Table 2	8 bits	8 bits	8bits See Equation 1	Xor(Command, Address,Data)

3.1.3 Write one row

Command	Row address	First bits of row	----	Last bits of row	Check
04_h	16 bits See Table 2	8 bits	8 bits	8bits See Equation 1	Xor(Command, Address,Data)

3.1.4 Clear screen (full black or full transparent)

Command	Check
19_h	Xor(Command,00_h)

Fill the display frame memory with '0'.

3.1.5 All pixels ON (full yellow)

Command	Check
$1A_h$	Xor(Command,00_h)

Fill the display frame memory with '1'.

3.1.6 Invert display image

Invert command only inverts visible display picture and does not manipulate picture data on display frame memory. Consecutive invert commands toggle displayed image between inverted and non-inverted mode.

Command	Check
$1C_h$	Xor (Command,00_h)

3.1.7 Write frame frequency

Relative Luminance	Command	Data	Check
100%[1)]	61_h	01_h	Xor (Command,Data)
75%	61_h	02_h	Xor (Command,Data)
50%	61_h	04_h	Xor (Command,Data)
30%	61_h	08_h	Xor (Command,Data)

Notes: [1)] Default luminance

3.1.8 Communication period

Display expects host to communicate periodically. If display does not receive a valid frame within a time period of about 1.5 seconds, the display is cleared to indicate that integrity of SPI bus may have been compromised or that host system may have malfunctioned. The timeout period is adjustable and can be entirely disabled if necessary.

Communication period	Command	Data	Check
Ab 1.5 sec [1)]	62_h	00_h	Xor (Command, Data)
Ab 3.0 sec	62_h	01_h	Xor (Command, Data)
-	-	-	
Ab 60 sec	62_h	27_h	Xor (Command, Data)
Disabled	62_h	$7F_h$	Xor (Command, Data)

Notes: [1)] Default time period

3.2 Display responding (MISO signal)

Displays were the MISO signal is implemented (see display manual) the display responds with command and check bytes.

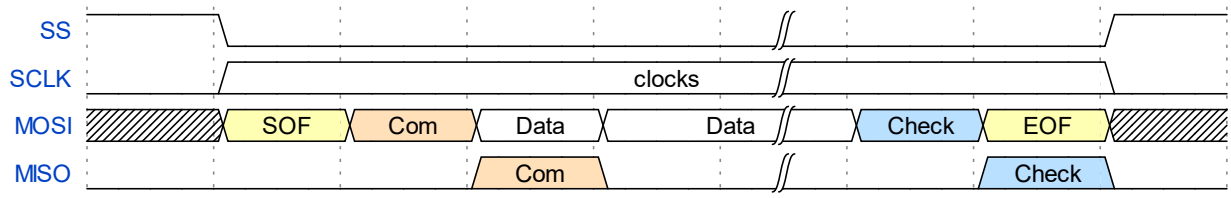

Figure 3. MISO Signal

3.3 SPI timing

The SPI is driven with the rising edge of SCLK. A falling edge on SS signal indicates the beginning of an access on the SPI, the rising edge of SS signal ends an access on SPI. An access must consist of exactly 8 bits for write operation.

It is preferable to keep SS signal constantly active throughout the entire write operation. Display can continue the transfer if SS signal is momentary driven to inactive state for short period of time. Successful continuation requires that clock pulse count and bit-based byte count remain in sync during the glitch.

The SPI interface Clock polarity (CPOL) and clock phase (CPHA) are 0. At CPOL=0 the base value of the clock is zero for CPHA=0 and data are captured on the clock's rising edge (low to high transition) and data is propagated on a falling edge (high to low clock transition).

The timing restrictions on SPI are defined in Figure 4 and Table 3:

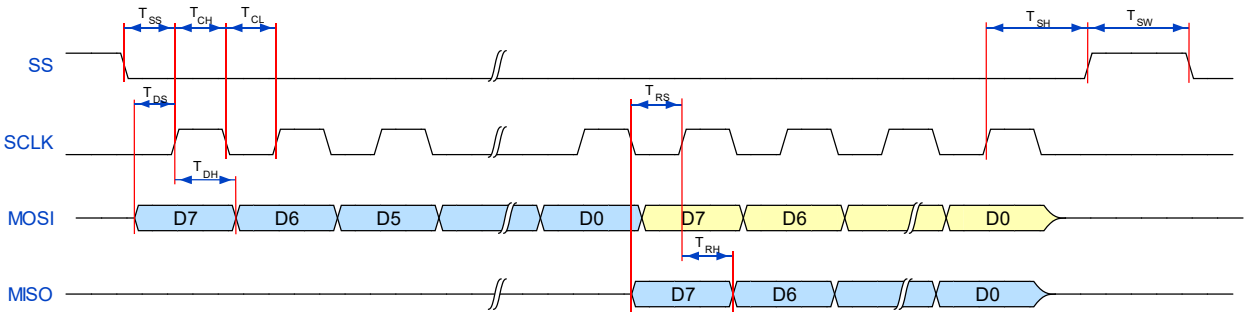

Figure 4. Video input timing diagram

Table 3. Timing restrictions

Description	Symbol	Minimum	Maximum	
SCLK frequency			5	MHz
SCLK high time	T_{CH}	100		ns
SCLK low time	T_{CL}	100		ns
SS -> SCLK setup time	T_{SS}	100		ns
SCLK -> SS hold time	T_{SH}	100		ns
SS disabled between cycles	T_{SW}	200		ns
Data setup time	T_{DS}	60		ns
Data hold time	T_{DH}	60		ns
Response Data setup time	T_{RS}	90		ns
Response Data hold time	T_{RH}	90		ns