



OVERVIEW

FEATURES

- 2 Analog Channels at up to 150 MHz Sample Rate per Channel
- 14 Bits of Resolution
- Bandwidth from 200 KHz to 200 MHz
- 512 Megabytes of On-Board Memory
- Compact ExpressCard design for Mobile Computer Applications
- Very low power consumption at less than 4.5W
- 266 MB/s PCIe Bus Implementation of ExpressCard
- PCIe Plug and Play Compatible Board

The EC14150 (EC) is a dual channel waveform capture board that provides a remarkable combination of high speed and high resolution sampling along with a very large memory capacity all in a very compact and low power consuming ExpressCard form factor. At 4.5 W, the EC represents one of the lowest power consuming digitizer cards ever created for its class. Signal frequencies up to 200 MHz can be accurately captured either in baseband or in higher order Nyquist zones using under-sampling techniques.

The EC is an ExpressCard 54 mm sized compliant board equipped with standard 'Plug and Play' features common in PCI systems. The entire 512 MB memory may be used as an exceptionally large FIFO for acquiring data directly to the ExpressCard bus continuously non stop (referred to as "EC Continuous Record Mode") or in the more simpler 2-step block acquisition to RAM and transfer to PC modes. In either the EC Continuous Record Mode (where the 512 RAM FIFO is used) or Data Transfer Mode; the EC card is capable of sustaining 180 megabyte/sec transfers over the ExpressCard bus interface. Significant test data has shown that recordings with this large 512 MB FIFO buffering the recording process can be continuous at up to 90 MSPS even when operating in traditional non real-time environments such as the Windows operating system.

APPLICATIONS

- SIGINT
- RADAR
- LIDAR
- Spectroscopy
- Mass Spectrometry – Time of Flight
- RF Communications
- Ultrasound
 - Medical Diagnostics
 - Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed / High Resolution Waveform Capture

The EC was designed to maximize the quality of the captured signal in terms of signal-to-noise ratio and spurious-free dynamic range over a very wide frequency range. A 24 dB amplifier/attenuator circuit is at the input of both analog channels, where 20 dB of amplification and 4 dB of attenuation are available for selection in steps of 1 dB. Both input channels implement a transformer coupled input for best possible signal performance.

A frequency synthesized clock allows the ADC sampling rate to be set to virtually any clock value up to 150 MHz, offering maximum flexibility for sampling rate selection. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, 5 PPM reference clock or to an externally provided 10 MHz reference clock via the onboard clock input connector. This same sync clock input connector can also be used for applying an external clock to the onboard EC ADCs.

The EC can be set to trigger from the input data channels, the external trigger signal input or via software command. The EC supports single shot, segmented, and pretrigger triggering modes.

HARDWARE DESCRIPTION

Overview

The block diagram below shows a simplified mechanization for the EC14150. The data input channels are AC coupled with a voltage range from 3 Vp-p at the high end and 100 mVp-p at the low end. There are a total of 24 voltage range settings between 3 V and 100 mV that can be selected for in 1 dB increments. At the amplifier/attenuator circuit output is a 200 MHz low pass filter to help reject higher frequency signals from aliasing into the data captured by the ADC. Customers can contact Signatec and request specific custom filter cutoff frequencies to optimize the EC14150 performance for their specific applications.

ADC data can be captured in dual channel or single channel mode. In single channel mode the entire signal memory can be used to capture data from channel 1 only.

The Pretrigger Samples FIFO can be thought of as a programmable length shift register with a maximum length of 4k samples and can be used to capture signal data before the trigger event. Before a trigger is received, the digitizers are active and data is continuously written into the shift register. After receiving a trigger, data samples are then written into the Acquisition FIFO. See the section “Trigger Modes and Options” for trigger mode details.

Data is written into the SDRAM via the Acquisition FIFO and read from RAM via the I/O FIFO. Advanced Signatec power management processes are implemented at this stage of memory management and controlling to meet a demanding 4.5 W power limit for ExpressCard based technologies.

Operating Modes

The EC14150 has 5 operating modes as follows:

1. Off – the EC14150 is powered down consuming very little power to conserve product life and mobile PC battery charge.
2. Standby – the only passive mode with no data activity.
3. RAM Acquisition – waveform data is captured into the on-board RAM.
4. EC Continuous Record – waveform data is passed to the ExpressCard PCIe bus, using the on-board 512 MBs of RAM as a FIFO.
5. EC PCIe Transfer – transfer data to the PCIe bus after a RAM Acquisition.

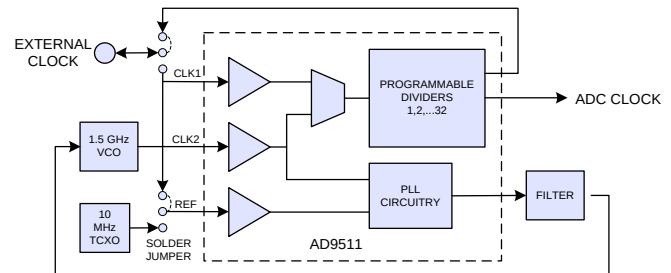
Of particular interest to most users is the EC Continuous Record mode, where the SDRAM is operated as a large FIFO for acquiring data directly to the ExpressCard PCIe bus. A large FIFO is necessary when acquiring large amounts of data to the PCIe bus in order to prevent data loss due to the host system's intermittent bus management activity. Data may be put into RAM at a maximum rate of 180 MB/s for a single channel while also being extracted at this same rate by interleaving the write and read data packets from the onboard EC14150 RAM. Due to power constraints of the ExpressCard form factor, only channel 1 at a maximum acquisition rate of 90 MHz is supported for the EC Continuous Record mode.

External Inputs/Outputs

Besides the signal data inputs, the EC14150 also provides MMCX connections for a clock or reference clock input and a trigger input. The clock input can be used to supply the source clock for the ADCs or a 10MHz reference clock for the internal synthesized clocks.

ADC Clock Circuit

An internal synthesized clock is the primary clock source for the ADCs. This synthesized clock on the EC14150 allows for users to dial in almost any frequency possible for the onboard ADCs with resulting sampling clock performance that matches or beats most fixed crystal oscillator performance. The ADC clock can also be supplied from the external clock input connector. The figure below shows the functionality of the ADC clock circuitry.



The synthesizer can generate any frequency from 45 to 128 MHz and most frequencies from 128 to 150 MHz. See the specification section for the range of un-settable frequencies.

If the external clock input is the ADC clock source, it may be divided by any integer value from 1 to 32.

For all clock sources the effective digitization rate can be further reduced via sample discarding of the digitized data. This second divider can be set from 2 to 32 in factors of 2.

When the synthesized clock is selected, ADC clock jitter is extremely low at about 200 fS RMS. The jitter is independent of the clock divider setting. Clock jitter can reduce the SNR of the captured signal at high frequencies.

The synthesizer clock is locked to a 10 MHz reference clock. The reference clock may be selected from the internal reference or an externally supplied reference clock. The internal reference clock is accurate to better than 5ppm. This sets the ADC clock accuracy to also be within 5ppm.

Triggering

The external trigger input can be used to synchronize the start of data acquisition with an external event. This is a digital input with TTL signal level. Triggering may be set to occur on either the positive or negative going edge of the signal.

Acquisition may also be set to occur based on the amplitude level of either of the two input signals exceeding a programmed trigger level.

The triggering threshold is a digital value that is compared against the digitized signal. The detection is edge based with either positive or negative excursion being selectable.

Trigger Modes and Options

In data acquisition mode, two triggering modes are available: single shot or segmented. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. The EC Continuous Record mode can be combined with the segmented trigger mode for creating high-speed continuous segment recordings.

HARDWARE DESCRIPTION (Continued)

Samples Settings

There are several board settings that affect the quantity and method of acquiring samples.

Active Memory Size – In the “post-trigger modes” this is the number of samples that will be taken after which the memory will be considered “full” and the acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt. The amount of memory that is activated for data acquisition may be set from 8 bytes to the full 512 megabytes in steps of 8 bytes. In EC Continuous Record mode it is also possible to operate in a “free run” mode whereby data is collected until the board is commanded to terminate the acquisition.

Segment Size – In Segmented Mode this is the number of samples that will be taken each time a valid trigger signal is detected.

Pretrigger Samples – In Single Shot or Segmented Modes, this is the number of samples that will be recorded into RAM that occurred before the trigger.

Delayed Trigger – This sets a delay between the actual applied trigger and the effective trigger for the board. The delay range is from 0 to 64k digitizer clock cycles.

ExpressCard PCIe Operation

The EC14150 implements a PCIe x1 lane version data link for the ExpressCard specification. This bus has a theoretical transfer bandwidth of up to 266 MB/s. In EC PCIe Transfer mode, the EC14150 will be capable of transferring data from the onboard RAM across this bus to the mobile PC RAM at a rate that is close to the 266 MB/s theoretical maximum (though this is PC dependant). Due to power restrictions, the long-term data-transfer rate over the ExpressCard PCIe bus in EC Continuous Record mode is limited to 90 MSPS (for single channel use only).

Under-Sampling and Anti-alias Filtering

The EC14150 has a maximum digitization rate of 150 MHz but has an analog bandwidth (filtered) of 200 MHz. The wide analog bandwidth provides the capability of acquiring signals at frequencies beyond the first Nyquist zone of the converter. Assuming a maximum digitizing rate of 150 MHz, the actual bandwidth of signals that can be captured is still limited to a maximum of 75 MHz but that band can be located anywhere in the 200 KHz to 200 MHz space, subject to the limitations imposed by the sampling frequency itself. Capturing signal frequencies that are more than one-half the sample rate is referred to as Under-Sampling.

At a sample rate of 100 MHz the EC14150 is capable of capturing 4 Nyquist zones (frequency bands, all numbers in Megahertz):

0 – 50	50 - 100	100 - 150	150 - 200
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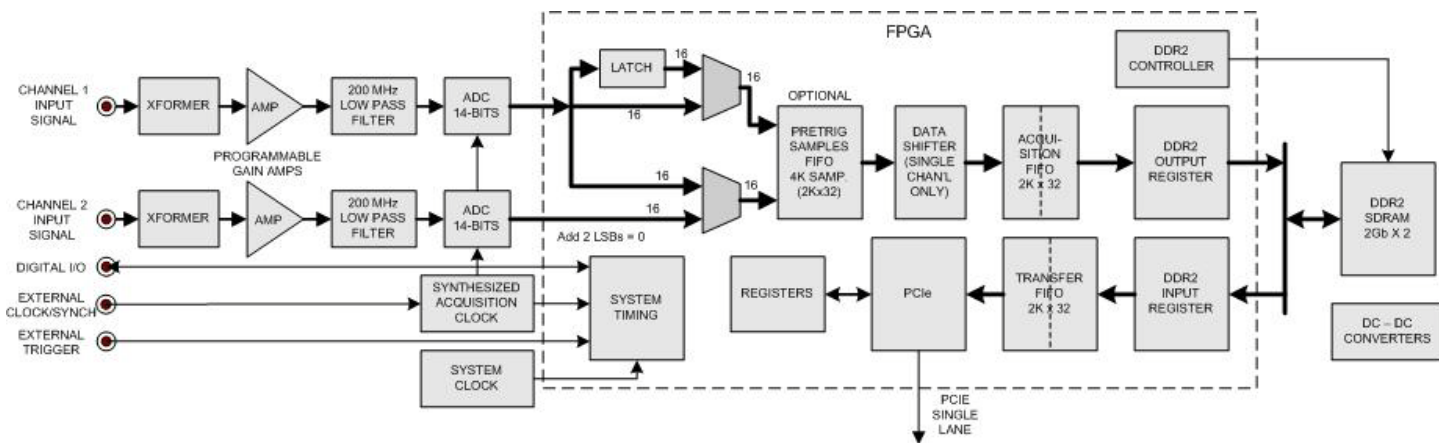
Operation in any of the frequency bands requires that signal frequencies from outside the band not be allowed to reach the ADC. This may involve the application of external band-pass filters to properly reject the out-of-band signals.

To capture frequency bands that span across two of the bands as shown in the table above, the ADC clock frequency would need to be reduced to shift the resulting Nyquist bands so as to completely capture the desired frequency range. Reducing the sampling frequency will reduce the bandwidth that can be captured.

Software

The EC14150 is supplied with the following software:

- Windows 2000/XP/Vista drivers
- C Function Library with source code
- Turnkey signal recording software application
- Software manual that describes how to use the available library of functions or API to create larger applications or systems.
- SDK offering many multiple coding examples



EC14150 Functionality Block Diagram

EC14150 SPECIFICATIONS AND ORDERING INFORMATION

External Signal Connections

Analog Input, Channel 1	: MMCX (miniature RF)
Analog Input, Channel 2	: MMCX
Clock Input	: MMCX
Trigger Input	: MMCX
Digital I/O	: MMCX

Analog Inputs

Full-Scale Volt. Ranges	: 100 mVp-p to 3 Vp-p (1 dB increments)
Impedance	: 50 ohms
Bandwidth	: 200 MHz (LP filter)
Coupling	: AC

External Trigger

Signal Type	: digital, TTL signal level
Impedance	: >10k ohms
Bandwidth	: 50 MHz

Internal Synthesized Clock

Frequency range	: 45.0 - 150 MHz
Resolution	: better than 5 PPM
Accuracy	: better than 5 PPM
Unsettable ranges	: 128.9-129.8, 140.6-142.8 MHz

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance	: 50 ohms
Frequency	: 10 MHz to 150 MHz
Amplitude	: 100 mV p-p to 2.0 V p-p

Post ADC Clock Divider

Divider Settings	: 1, 2, 4, 8, 16, 32
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Reference Clock

Internal	: 10.0 MHz, ± 5 ppm max.
External	: 10.0 MHz, ± 50 ppm max (required for lock)

Digitizer

Resolution	: 14 bits
Aperture Jitter	: 0.07 pS typical
Clock Rate	: 45 to 150 MHz

Trigger Modes

Post Trigger	: single start trigger fills active memory
Pretrigger	: single trigger stops acquisition
Segmented	: start trigger for each memory segment

Trigger Options

Pretrigger Samples	: samples prior to trigger are stored; Single Channel: 8k max.; Dual Channel: 4k max per channel
Delayed Trigger	: delay from trigger to data storage; Up to 64k digitizer clock cycles

Memory

Active Size	: Up to 256 MegaSamples
Segment Size	: Up to 128 Megasamples
Segment re-arm time ¹	: 150 nanoseconds
Addressing	: DMA transfer from starting address

I/O Addressing

PCI Controller Address	: 64 bytes, Plug and Play selected
Control/Status Registers	: 32 bytes, Plug and Play selected

Performance

SFDR	: 80dB, 1 to 50 MHz
	: 78dB @ 100 MHz
	: 77dB @ 170 MHz
SNR (1-200 MHz)	: 67dB @ 20dB gain
	: 66dB @ 10dB gain
	: 65dB @ 0dB gain

Power Requirements

+3.3V	: 1.5 Amps max.
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Absolute Maximum Ratings

Analog Inputs	: ± 5 volts
Trigger Input	: -0.2 to +4.0 volts DC
Clock Input	: 5 volts peak to peak
Ambient Temperature	: 0 to 50 C

Definition of Terms

SNR: Signal to Noise Ratio - The ratio of the fundamental sinusoidal power to the noise power. For this data sheet, noise power is considered to be the power from all spectral components with the exception of the fundamental signal, the first harmonic, and the second harmonic.

SFDR: Spurious Free Dynamic Range - The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

EC14150 Part Numbers

EC14150-[LPF]

[LPF] = Cutoff frequency for the low pass filter in MHz. Standard is a 200 MHz LPF. Specify other values for custom filters. For no upper cutoff, this [LPF] should be 0.

Example Part Order Numbers:

EC14150 (Standard 200 MHz Low-pass Filter)

EC14150-75 (75 MHz Low-pass Filter)

Documentation & Accessories

The EC14150 is supplied with a comprehensive operator's manual, which thoroughly describes the operation of both the hardware and the software. Also supplied are two four-foot coaxial cables with MMCX to BNC connectors. Additional cables may be purchased. Supplied software disks contain a function library for Microsoft Visual C/C++, example programs, and all source code to libraries and examples.

Product Warranty

All Signatec products carry a full 1-year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. This warranty does not cover customer misuse or abuse of the products or physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:

1. In segmented mode, time from the end of a segment until a trigger will be accepted to begin another segment acquisition.

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

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