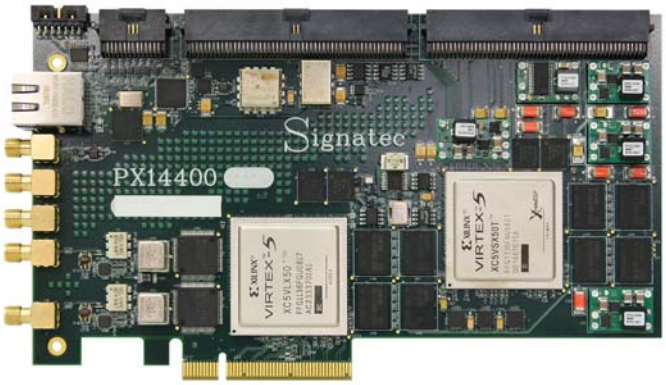
Product Information Sheet

PX14400A

2 Channel, AC-Coupled, 14-Bit Digitizer



FEATURES

- 2 Analog Channels at up to 400 MHz Sample Rate per Channel
- 14 Bits of Resolution
- Bandwidth from 100 KHz to 400 MHz
- 1 GB RAM (512 MB for Raw Data Capture / 512MB for FPGA Processing)
- 1400 MB/s Continuous Transfer Over PCI Express Bus (8 lanes)
- Xilinx Virtex-5 FPGAs
- Available Product Options:
  - 10/100/1000 Ethernet Port
  - Onboard Customer Programmable FPGA
  - Ample Support for User HW and SW Customized Processing Functionality
  - Xilinx Compatible JTAG Port Simplifies Development of User FPGA Processing

APPLICATIONS

- SIGINT
- RADAR
- LIDAR
- Spectroscopy
- Mass Spectrometry – Time of Flight
- RF Communications
- Ultrasound
  - Medical Diagnostics
  - Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed / High Resolution Waveform Capture

OVERVIEW

The PX14400A is a dual channel AC-coupled waveform capture board that provides a remarkable combination of high speed and high resolution sampling along with a very large memory capacity. Signal frequencies up to 200 MHz can be accurately captured when using the programmable gain amplifier or up to 400 MHz if the direct transformer coupled connection is used.

The PX14400A has a primary sample-data RAM bank of 512 MB memory that may be used as an exceptionally large FIFO for acquiring non-stop, continuous data directly to either the PCI Express (PCIe) bus or the SAB. In Buffered Acquisition Mode (where the 512 MB RAM FIFO is used) the PX14400A is capable of sustaining 1400 MB/s over the PCIe bus. Significant test data has shown that recording with large FIFO buffering can be continuous at these rates even when operating in traditional non real-time environments such as the Windows operating system.

The PX14400A employs up to two Virtex-5 FPGAs, where one of the FPGAs is available as an option for customers to implement their own custom in-line signal processing. A standard FIFO interface to the Signatec specific logic portion of the PX14400A along with control flags, an example program using the FIFOs/flags and a programmer's manual are provided with the optionally available PX14400A Firmware Development Kit. The PX14400A can be ordered either with or without this 2nd user accessible FPGA. Boards without the user FPGA are -DR (data recording only) models and boards with the user FPGA are -SP (signal processing) models.

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The PX14400A was designed to maximize the quality of the captured signal in terms of signal-to-noise ratio and spurious-free dynamic range over a very wide frequency range. The programmable amplifier allows for setting the full scale input voltage from 220 millivolts to 3.5 volts in 1 dB steps.

A frequency synthesized clock allows the ADC sampling rate to be set to virtually any value from 20 to 400 MHz (except 277 MHz to 308 MHz), offering maximum flexibility for sampling rate selection. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, 5 PPM reference clock or to an externally provided 10 MHz reference clock. The ADC may also be clocked from an external clock source.

Up to five PX14400A boards may be interconnected in a Master/Slave configuration via a ribbon cable that connects at the top of the board. In this configuration, the Master board drives the clock and trigger signals for the Slave boards so that data sampling on all boards occurs simultaneously. Additional boards can be synchronized, either within a single PC chassis or across multiple PC chassis, by adding the optional SYNC1500-6 product as the clock and trigger source for the system.

HARDWARE DESCRIPTION

Analog Input Section

The block diagram shows a simplified mechanization for the PX14400A. The input signals are AC coupled. The board must be set at the factory for either direct transformer coupled input or input via the programmable gain amplifier.

The transformer input allows for higher frequency operation as well as slightly better performance in terms of SNR and SFDR, but this higher performance comes at the cost of a fixed gain input.

The amplifier allows for setting the full-scale input voltage range from 220 millivolts to 3.5 volts. The gain of the amplifier is set via a 5-bit digitally controlled attenuator. The amplifier drives a 200 MHz 3-pole Bessel filter, which has the characteristic of a flat (constant) time delay response over the frequency range.

Data Management

ADC data can be captured in dual channel or single channel mode. The onboard memory is not dedicated to a particular channel resource, so in single channel mode the entire signal memory can be used to capture data from channel 1 only.

The PX14400A can be programmed to acquire a programmable amount of pretrigger samples. Conversely, it can also be programmed to acquire samples using a delayed trigger. See the section "Trigger Modes and Options" for trigger mode details.

Operating Modes

The PX14400A has 4 standard operating modes as follows:

1. Standby – the only passive mode with no data activity
2. RAM Acquisition – waveform data is captured into the on-board RAM
3. PCIe Buffered Acquisition – waveform data is passed to the PCIe bus, using 512 MBs of onboard RAM as a FIFO
4. PCIe Transfer – transfer data to the PCIe bus after a RAM Acquisition

The PX14400A has 4 additional operating modes when using signal processing enabled versions of the PX14400A, which are as follows:

5. SAB Transfer – transfer data to SAB after a RAM Acquisition
6. SAB Acquisition – waveform data is passed to SAB bus, bypassing the on-board RAM
7. SP PCIe Buffered Acquisition – same as standard PCIe Buffered Acquisition, but with data routed to 2nd FPGA for data processing before transfer to PCIe
8. SP SAB Acquisition – same as standard SAB Acquisition, but with data processing before transfer to SAB

Of particular interest are the 2 versions of the PCIe buffered acquisition modes, where the SDRAM is operated as a large FIFO for acquiring data to the PCIe bus. Data may be put into RAM at a maximum rate of 1600 MB/s (2 channels at 400 MHz) while also being extracted at this same rate by interleaving write and read data packets, though the transfer to PCIe is limited to 1400 MB/s maximum. Acquisitions at the full 1600 MB/s are possible when data processing is used and results are reduced to 1400 MB/s or less.

Triggering

The external trigger input can be used to synchronize the start of data acquisition with an external event. This is a digital input with TTL signal level. Triggering may be set to occur on either the positive or negative going edge of the signal.

Acquisition may also be set to occur based on the amplitude level of either of the two input signals exceeding a programmed trigger level. The triggering threshold is a digital value that is compared against the digitized signal. The detection is edge based with either positive or negative excursion being selectable.

Trigger Modes and Options

In any of the data acquisition modes, two triggering modes are available: single shot or segmented. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. The PCIe buffered acquisition modes can be combined with the segmented trigger mode for creating high-speed continuous segment recordings.

Time Stamps

In Segmented Mode, "time stamps" allow for storing the time relationship between the memory segments. Time Stamps are 32 bit timer values with a clock resolution of 5.0 nanoseconds, and are accumulated in a 2048 element FIFO memory separate from the data. If necessary, time stamps may be read during acquisition in order to prevent overflow. This is possible in any acquisition mode.

Samples Settings

There are several board settings that affect the quantity and method of acquiring samples.

Active Memory Size – This is the number of samples that will be taken after which the memory will be considered "full" and the acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt or send an interrupt over the SAB. The amount of memory that is activated for data acquisition may be set from 8 bytes to the full 512 megabytes in steps of 8 bytes. In buffered acquisition modes it is also possible to operate in a "free run" mode whereby data is collected until the board is commanded to terminate the acquisition.

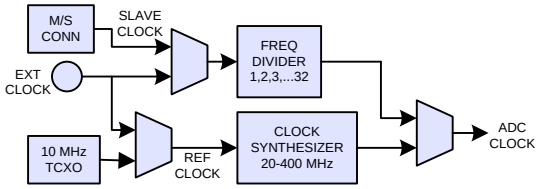
Segment Size – In Segmented Mode this is the number of samples that will be taken each time a valid trigger signal is detected.

Pretrigger Samples – This is the number of samples that will be recorded into RAM that occurred before the trigger.

Delayed Trigger – This sets a delay between the actual applied trigger and the effective trigger for the board. The delay range is from 0 to 64k digitizer clock cycles. In Pretrigger Samples mode the delayed trigger setting establishes the number of post-trigger samples that will be recorded.

ADC Clock Circuit

An internal synthesized clock is the primary clock source for the ADCs. This synthesized clock on the PX14400A allows for users to dial in almost any frequency possible for the onboard ADCs with resulting sampling clock performance that matches or beats most fixed crystal oscillator performance. The ADC clock can also be supplied from the external clock input or from the Slave clock at the Master/Slave connector. The figure below shows the functionality of the ADC clock circuitry.



The synthesizer can generate most frequencies from 20 to 400 MHz. See the specification section for the range of un-settable frequencies.

If the external clock input is the ADC clock source, it may be divided by any integer value from 1 to 32. For Master/Slave board combinations the slave board(s) derive(s) the ADC clock from the Master/Slave connector via a ribbon cable connection. For slave boards the frequency divider should be set to 1 to match the slave clock to the master clock.

For all clock sources the effective digitization rate can be further reduced via sample discarding of the digitized data. This second divider, located inside the System FPGA, can be set from 2 to 32 in factors of 2.

The synthesizer clock is locked to a 10 MHz reference clock. The reference clock may be selected from the internal reference or an externally supplied reference clock. The internal reference clock is accurate to better than 5ppm. This sets the ADC clock accuracy to also be within 5ppm.

Under-Sampling and Anti-alias Filtering

The PX14400A has a maximum digitization rate of 400 MHz which allows for capturing up to 200 MHz of bandwidth. If capturing signals above 200 MHz is required then the transformer connected front end must be selected. Capturing signal frequencies that are more than one-half the sample rate is referred to as Under-Sampling. In this case the board would acquire data in the second Nyquist zone.

Operating in this manner requires that signal frequencies from outside the band not be allowed to reach the ADC. This may involve the application of external band-pass filters to properly reject the out-of-band signals.

To capture a particular frequency band it may be necessary to reduce the ADC clock frequency so as to shift the resulting Nyquist bands to completely capture the desired frequency range. Reducing the sampling frequency will reduce the bandwidth that can be captured.

External Inputs/Outputs

Besides the signal data inputs, the PX14400A also provides SMA connections for a clock input, a trigger input, and a digital input/output signal. The clock input can be used to supply the source clock for the ADCs or a 10MHz reference clock for the internal synthesized clocks. Ethernet connectivity is also available as an option.

The digital I/O connector will typically be used for outputting clock and trigger signals but it can also be reprogrammed to provide custom capabilities as either an input or an output.

SAB Operation

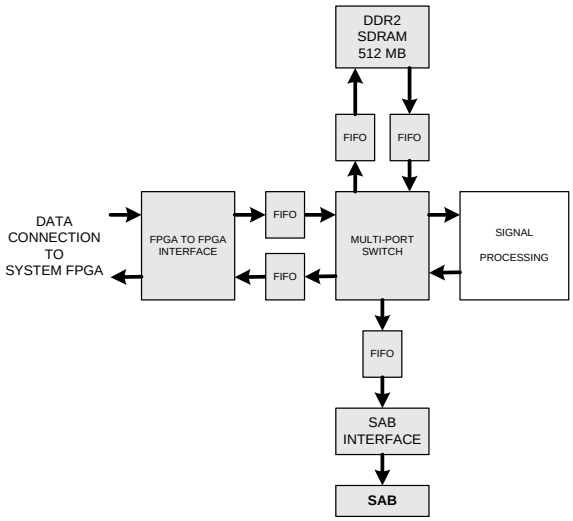
The PX14400A can perform SAB data transfers (as an option) at 64 bits, or at 32 bits over either the high (SABH) or low (SABL) bus ports. This provides flexibility when multiple boards are incorporated into a system.

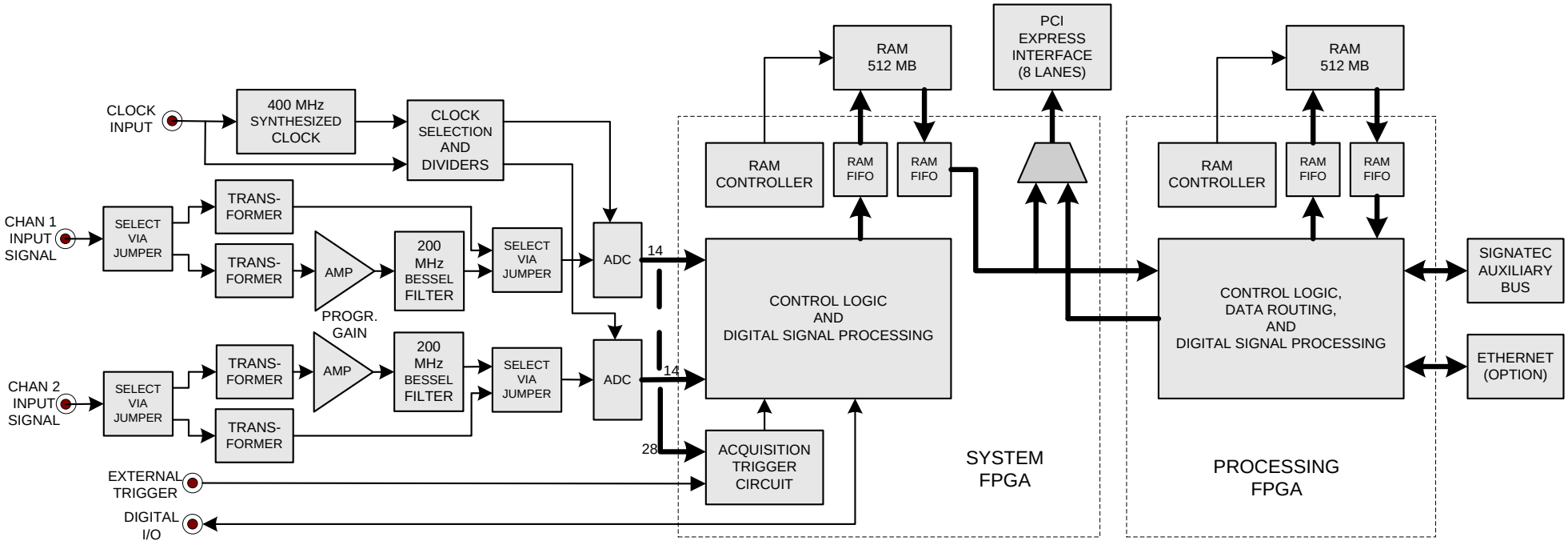
PCIe Operation

The PX14400A is capable of sustaining a long-term data-transfer rate, over the PCIe bus, of about 1400 megabytes per second. This is slightly less than the full acquisition data rate of 1600 MB/s. For long term operation the output data rate limit can be met by reducing the sample rate or by performing data reduction via data processing. A simple mechanization would be to pack the output data into 12 or 14 bit format.

Onboard FPGA Signal Processing (*Option)

The block diagram below shows the data flow within the optionally available signal processing FPGA. A firmware development kit (not included with the PX14400A hardware) can be purchased with the product, which demonstrates how to write real-time FPGA programs for the PX14400A board. The provided example demonstrates how to utilize the various FIFO, RAM, processing elements and bus interface resources shown below. Signatec also offers design services for customers who don't wish to program the FPGA themselves. Contact Signatec Sales for more details.





PX14400A FUNCTIONALITY

SOFTWARE / ATTENUATORS

Software

The PX14400A is supplied with the following software:

- Windows 32-bit & 64-bit drivers
- Linux 32-bit & 64-bit drivers
- C/C++ Callable Function Library or API for custom software development
- Turnkey signal recording software application for Windows
- Software manual that describes the PX14400A and information for using the available library of functions or API
- SDK offering multiple coding examples for PC side applications

The PX14400A has the following optional software/firmware packages:

- Signal monitoring software, with real-time FFT, FIIR filtering, DDC and data recording capabilities for Windows
- FPGA processing packages with fixed capabilities for FFT, FIIR filtering and DDC real-time processing
- FPGA Development Kit package for customer programming
- LabVIEW Interface package with supplied VIs, software development kit and manual

DEFINITION OF TERMS

SNR: Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power. For this data sheet noise is considered to be the power from all spectral components except for the fundamental signal, the first harmonic, and the second harmonic.

SFDR: Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

Attenuators

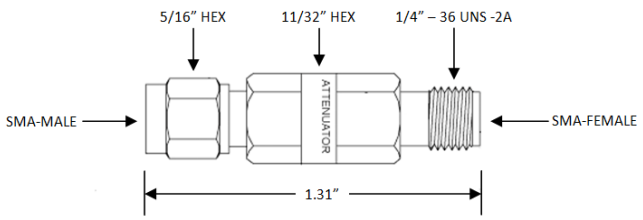
To order optional SMA attenuators for use with the PX14400A, use the following part number:

SMA Attenuator Part Number: **662-*dB*-1**

Insert the attenuation value in place of ***dB***.

EXAMPLE: 662-**6**-1 for **6 dB**

The attenuator specifications are as follows:



ELECTRICAL SPECIFICATIONS					
Avg. Power (Watts)	Peak Power (Watts)	Freq. (GHz)	VSWR (Max)	Attenuation Value (dB)	Attenuation Tolerance
2	500	Hz-2.0 2.0-4.0	1.15:1 1.25:1	3, 6, 10, 20 dB	± 0.6 dB ± 0.8 dB
		Hz-2.0 2.0-4.0	1.25:1 1.35:1	30 dB**	± 1.0 dB ± 1.5 dB

** All other Values from 1-32 dB follow 30dB specs

MECHANICAL SPECIFICATIONS	
Connectors:	Brass Albaloy Plated
Male Pin:	Brass Gold Plate
Female Pin:	Beryllium Copper Gold Plate
Housing:	Brass Albaloy Plate
Insulator:	PTFE Virgin Electrical Grade
Operating Temperature:	-67° F to +185° F -55° C to +85° C
Weight:	62 oz 1.76 kg

PX14400A SPECIFICATIONS AND ORDERING INFORMATION

External Signal Connections

Analog Input, Channel 1	: SMA
Analog Input, Channel 2	: SMA
Clock Input	: SMA
Trigger Input	: SMA
Digital Input / Output	: SMA

Analog Inputs – Amplifier

Full Scale Volt. Ranges	: 220 mV to 3.5 V in 1dB steps
Impedance	: 50 ohms
Bandwidth	: 100kHz - 200 MHz (Bessel filter)
SNR (1-200 MHz)	: 65 dB
SFDR (@ 100 MHz)	: 83 dB

Analog Inputs - Transformer

Full Scale Input Voltage	: 1.1 Volts
Impedance	: 50 ohms
Bandwidth	: 500 kHz to 400 MHz
SNR (1-200 MHz)	: 68 dB
SFDR (@100 MHz)	: 80 dB

External Trigger

Signal Type	: digital, TTL signal level
Impedance	: >10k ohms
Bandwidth	: 50 MHz

Internal Synthesized Clock

Frequency range	: 20.0 - 400 MHz
Resolution	: better than 10 PPM
Accuracy	: better than 5 PPM
Unsettable range	: 277-308 MHz

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance	: 50 ohms
Frequency	: 20 MHz to 400 MHz
Amplitude	: 100 mV p-p to 2.0 V p-p

Post ADC Clock Divider

Divider Settings	: 1, 2, 4, 8, 16, 32

Reference Clock

Internal	: 10.0 MHz, ± 5 ppm max.
External	: 10.0 MHz, ± 50 ppm max (required for lock)

Digital Input / Output

Type	: TTL Logic Level (standard)
Max. Frequency	: 200 MHz
Connection	: 50 ohms to FPGA I/O

Trigger Modes

Post Trigger	: single start trigger fills active memory
Pretrigger	: single trigger stops acquisition
Segmented	: start trigger for each memory segment

Trigger Options

Pretrigger Samples	: samples prior to trigger are stored; Single Channel: 8k max.; Dual Channel: 4k max per channel
Delayed Trigger	: delay from trigger to data storage; Up to 64k digitizer clock cycles

Memory

Total Size	: 512 Megasamples; split 50/50 for raw sample data capture and FPGA data processing
Segment Size	: Up to 128 Megasamples
Segment re-arm time	: 150 nanoseconds
Addressing	: DMA transfer from starting address

Signatec Auxiliary Bus (Version 4)

Data Transfer Rates	: TBD
Data Direction	: output only

Power Requirements

+12V	: 1.0 Amps max.
+3.3V	: 3.3 Amps max.

Absolute Maximum Ratings

Analog Inputs	: ±4 volts
Trigger Input	: -0.2 to +4.0 volts DC
Clock Input	: 5 volts peak to peak
Operating Temperature	: +32°F to +122°F 0°C to 50°C
Storage Temperature	: -4°F to +158°F -20°C to +70°C
Operating Relative Humidity	: 10% to 90%, non-condensing
Operating Vibration	: 0.25 G, 5 Hz to 500 Hz
Operating Shock	: 2.5 G, 11 ms, ½ sine
Board Dimensions	: 7.5” L x 4.3” H x 0.75” W 19.0cm L x 10.9cm H x 1.9cm W

Part Numbers and Ordering Information

The PX14400A has the following part number modifiers that determine the configuration of the board. These are as follows:

-DR	: No User Programmable FPGA
-SP50	: V5 SX50T Sized User Programmable FPGA
-SP95	: V5 SX95T Sized User Programmable FPGA
-AMP-200	: Amplifier Front End with Default 200MHz Low Pass Filter
-XF-400	: Transformer Front End with Default 400MHz Bandwidth
-MS	: Configured for Master/Slave Operation
-SY	: Configured for Master/Slave Operation with SYNC1500-6

The PX14400A part number nomenclature is as follows:

PX14400A-[DR or SP50 or SP95]-[AMP-200 or XF-400 or opt filter mod]-[opt MS or SY]

Example: **PX14400A-SP50-AMP-200-MS** would call for a PX14400A board with the Virtex 5 SX50T sized user programmable FPGA, the amplifier signal input path with default 200MHz Low Pass Filter, and master/slave configuration. Please contact Signatec for optional filter modifications. The master/slave modifiers “MS” or “SY” are not required for standalone operation of individual boards, and should only be included in the ordering part number when planning to use multiple boards together for synchronized multi-board channel operations.

SAB Cables

Refer to the “SAB Cable Assembly Ordering Guide” to select and order the appropriate cable assemblies if required.

Attenuators

Refer to Attenuators section on Page 5 of this data sheet.

Documentation & Accessories

The PX14400A is supplied with a comprehensive operator’s manual, which thoroughly describes the operation of both the hardware and the software. Also supplied are two four-foot coaxial cables with SMA to BNC connectors. Additional cables may be purchased. Supplied software disks contain a function library for Microsoft Visual C/C++, example programs, and all source code to examples.

Product Warranty

All Signatec products carry a standard full 1-year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. Optional Extended Warranty Plans are also available for purchase for up to a maximum 5-year warranty period. Standard and Optional Extended Warranties do not cover customer misuse or abuse of the products or physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

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