

**FEATURES**

- 4 Analog Channels at up to 1500 MHz Sample Rate per Channel at 8 Bits Resolution
- 2 Analog Channels at up to 3000 MHz Sample Rate per Channel in Interleaved Mode
- Bandwidth up to 2 GHz
- 2 Gigabytes of On-Board Memory
- 1400 MB/s Continuous Transfer Over PCI Express Bus (8 lanes)
- Xilinx Virtex-5 FPGAs
- User Application Support:
 - Onboard Customer Programmable FPGA
 - Ample Support for User HW and SW Customized Processing Functionality
 - Xilinx Compatible JTAG Port Simplifies Development of User FPGA Processing

APPLICATIONS

- SIGINT
- RADAR
- LIDAR
- Spectroscopy
- Mass Spectrometry – Time of Flight
- RF Communications
- Ultrasound
 - Medical Diagnostics
 - Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed / High Resolution Waveform Capture

OVERVIEW

The PX1500-4 is a four channel waveform capture board that can acquire up to 1500 MSPS on each channel or up to 3000 MSPS for dual channel operation when ADC data is interleaved. The PX1500-4 can be set up to use either a transformer coupled front end or an amplifier connection. The transformer connection has a frequency capture range of 5 MHz to 2 GHz. The amplifier can be set for either AC or DC coupled operation with a frequency range of up to 1 GHz.

The board features an 8 lane PCI Express connection to the computer host as well as 2 gigabytes of on-board memory. If the average acquisition data rate does not exceed 1400 MB/s then the entire 2 GB memory may be used as an exceptionally large FIFO for acquiring non-stop, continuous data directly to the PCI Express bus. Significant test data has shown that recording with large FIFO buffering can be continuous at these rates even when operating in traditional non real-time environments such as the Windows operating system.

The PX1500-4 employs two Virtex-5 FPGAs which have ample unused programmable logic cells for customers to implement their own custom in-line signal processing (as an option). Hooks and examples are provided to simplify this task.

The PX1500-4 was designed to maximize the quality of the captured signal in terms of signal-to-noise ratio and spurious-free dynamic range over a very wide frequency range. The programmable amplifier allows for setting the full scale input voltage from 200 millivolts to 3.0 volts in 1 dB steps.

A frequency synthesized clock allows the ADC sampling rate to be set to virtually any value from 200 MHz, the minimum allowable ADC clock, to 1500 MHz, offering maximum flexibility for sampling rate selection. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, 5 PPM reference clock or to an externally provided 10 MHz reference clock. The ADC may also be clocked from an external clock source.

Up to three PX1500-4 boards may be interconnected in a Master/Slave configuration via a ribbon cable that connects at the top of the board. In this configuration the clock and trigger signals from the Master drive the Slave boards so that data sampling on all boards occurs simultaneously. Up to six boards can be set up for fully synchronized operation by utilizing the SYNC1500-6 as the clock and trigger source for the system.

HARDWARE DESCRIPTION

Analog Input Section

The analog input circuitry for each of the four channels is identical. The four channels are designated as I1, Q1, I2, and Q2. The board can be set up to use either a transformer coupled front end or an amplifier connection. The transformer input allows for higher frequency operation, up to 2 GHz, as well as slightly better performance in terms of SNR and SFDR. The amplifier provides the ability to capture lower frequencies and operate at lower signal levels.

Data Flow

The block diagram on page 4 shows how the data flows through the system. In normal operation, data flows through the various circuit functions via a series of self-managed FIFO to FIFO transfers. Processing functions can be inserted into the data flow as shown. These can be either Signatec supplied or User derived.

Operating Modes

The PX1500-4 has 7 operating modes as follows:

1. Standby – the only passive mode with no data activity.
2. RAM Acquisition – waveform data is captured into the on-board RAM.
3. PCI Acquisition – waveform data is passed to PCI bus, bypassing the on-board RAM (limited to small acquisition sizes).
4. PCI Buffered Acquisition – waveform data is passed to the PCI bus, using the on-board RAM as a very large FIFO.
5. SAB Acquisition – waveform data is passed to SAB bus, bypassing the on-board RAM. (Option)
6. PCI Transfer – transfer data to the PCI bus after a RAM Acquisition.
7. SAB Transfer – transfer data to the SAB bus after a RAM Acquisition. (Option)

Of particular interest is the PCI buffered acquisition mode, where the SDRAM is operated as a large FIFO for acquiring data directly to the host system memory via the PCI Express bus. A large FIFO is necessary when acquiring large amounts of data to the PCIe bus in order to prevent data loss due to the host system's intermittent PCIe bus activity.

Triggering

The external trigger input can be used to synchronize the start of data acquisition with an external event. In order to support precise, high speed triggering, this signal is a LVPECL input that is terminated with 50 ohms to +1.3 volts. This is the proper termination for a LVPECL signal source based on +3.3V VCC. The trigger occurs on the positive going edge.

Precise, synchronized triggering of multiple PX1500-4 boards can be obtained by connecting up to three boards in a master/slave connection whereby the master board provides the trigger, clock, and sync signals for one or two slave boards. The master/slave connection is made via a ribbon cable across the top of the boards.

Up to six PX1500-4 boards can be operated in synchronization when driven by the SYNC1500-6 Clock and Trigger board. This provides the very precise clock, trigger, and sync signals for all six boards.

Acquisition may also be set to occur based on the amplitude level of the signal on input channel I1. Both a high level and a low level threshold may be set up. The triggering thresholds are digital values that are compared against the digitized signal. Triggering can be set to occur when the signal exceeds either the high level or low level threshold.

Trigger Modes and Options

In data acquisition mode, two triggering modes are available: single shot or segmented. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. The PCI buffered acquisition mode can be combined with the segmented trigger mode for creating high-speed continuous segment recordings.

Time Stamps

In Segmented Mode “time stamps” allow for storing the time relationship between the memory segments. Time Stamps are 64 bit timer values with a clock resolution of $4/f_{ADC}$, and are accumulated in a 2048 element FIFO memory separate from the data. If necessary, time stamps may be read during acquisition in order to prevent overflow. This is possible in any acquisition mode.

Samples Settings

There are several board settings that affect the quantity and method of acquiring samples.

Active Memory Size – This is the number of samples that will be taken after which the memory will be considered “full” and the acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt or send an interrupt over the SAB. The amount of memory that is activated for data acquisition is programmable up to 2 Gigabytes in steps of 16 bytes. In buffered acquisition modes it is also possible to operate in a “free run” mode whereby data is collected until the board is commanded to terminate the acquisition.

Segment Size – In Segmented Mode this is the number of samples that will be taken each time a valid trigger signal is detected.

Pretrigger Samples – This is the number of samples that will be recorded into RAM that occurred before the trigger.

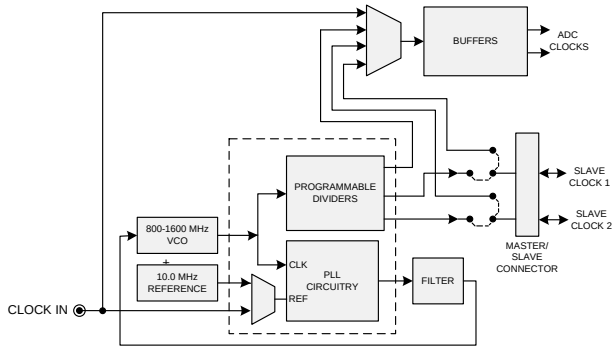
Delayed Trigger – This sets a delay between the actual applied trigger and the effective trigger for the board. The delay range is from 0 to 64k digitizer clock cycles. In Pretrigger Samples mode the delayed trigger setting establishes the number of post-trigger samples that will be recorded.

HARDWARE DESCRIPTION (CONTINUED)

ADC Clock Circuit

A functional pictorial for the PX1500-4 clock circuitry is shown in the figure below. The ADC clocks can be selected from one of four sources; an external clock, an internal synthesized clock, or 1 of the 2 slave clock inputs.

The internal synthesized clock is the primary clock source for the ADCs. The synthesized clock can generate any clock frequency from 200 to 1500 MHz to a resolution of 62 ppm or better.



For all clock sources the effective digitization rate can be further reduced via sample discarding of the digitized data. This second divider, located inside the System FPGA, can be set from 2 to 32 in factors of 2.

The synthesizer clock is locked to a 10 MHz reference clock. The reference clock may be selected from the internal reference or an externally supplied 10 MHz reference clock. The internal reference clock is accurate to better than 5ppm. This sets the ADC clock accuracy to also be within 5ppm.

Interleaved Clocking

The PX1500-4 can be set to perform interleaved clocking. In this mode the signal from one of the ADC inputs is sampled by both ADCs in the same package, but on the opposite edges of the sampling clock. In this mode the sample rate can be as high as 3.0 GHz. This allows for capturing a full 1500 MHz of bandwidth. The number of input channels is reduced to two in this mode.

Sync Input

A sync signal is required to synchronize the ADCs on multiple PX1500-4 boards. If two or three boards are connected in a master/slave group, the sync signal is provided by the master board over the master/slave cable. If more than three boards are to be synchronized, the external clock and trigger board (SYNC1500-6) should be used. It will provide clock, trigger, and sync signals over coaxial cables via the PX1500-4 SMA connectors.

SAB Operation

The PX1500-4 can perform SAB data transfers at 64 bits, or at 32 bits over either the high (SABH) or low (SABL) bus ports. This provides a simple data transfer protocol for moving data to user specific hardware. The SAB operation for the PX1500-4 is currently an option feature.

PCI Express Operation

The PX1500-4 is capable of sustaining a long-term data-transfer rate, over the PCIe bus, up to 1400 megabytes per second. If the average input data rate does not exceed this rate then PCI Buffered Acquisition mode can be utilized to stream long-term, uninterrupted data flow to the PC. The average input data rate can be reduced via any combination of the following:

1. Reducing the ADC sample rate;
2. Using fewer input data channels;
3. Using Segmented Data Acquisition.

Very-high-speed RAID systems are available that can store data indefinitely at a 1400 MB/s rate.

Signal Processing

The block diagram on the next page shows where signal processing functions can be dropped into the data flow paths. Firmware development kits are available from Signatec as an option for either fixed real-time processing capabilities or for custom programming by the user. Packages that allow for custom programming include source code examples along with a programmer's manual. Customers creating custom logic for the PX1500-4 FPGAs will require Xilinx ISE software version 10 or higher.

Software

The PX1500-4 is supplied with the following software:

- Windows 32-bit & 64-bit drivers
- Linux 32-bit & 64-bit drivers (Not yet available)
- C/C++ Callable Function Library
- Turnkey signal recording software application
- Software manual that describes the PX1500-4 and information for using the available library of functions or API
- SDK offering multiple coding examples for PC side applications

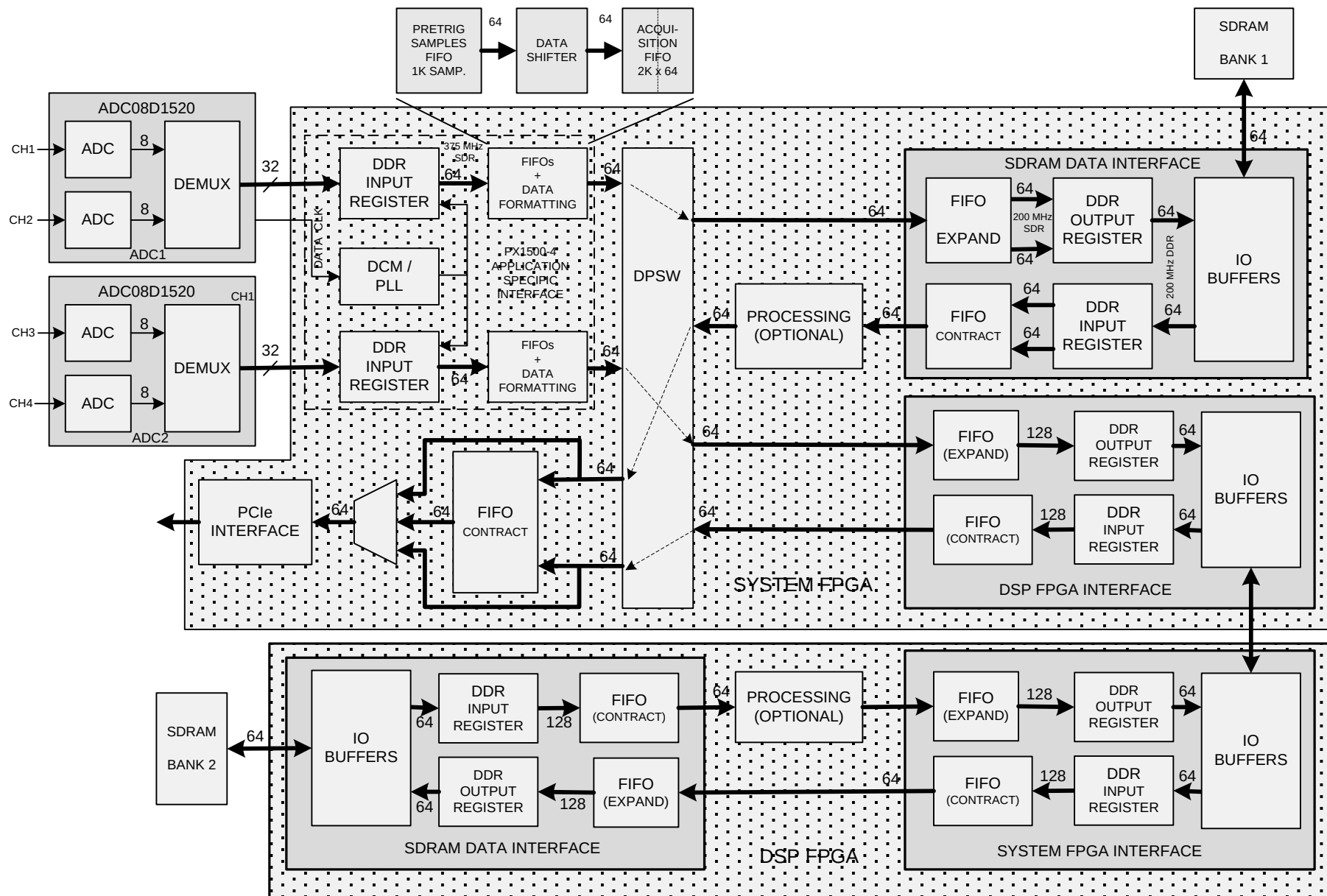
The PX1500-4 has the following optional software/firmware packages:

- Signal monitoring software, with real-time FFT, FIIR filtering, DDC and data recording capabilities
- FPGA processing packages with fixed capabilities for FFT, FIIR filtering, DDC real-time processing
- FPGA package for customer programming
- LabVIEW driver, VIs, software development kit and manual (Not yet available)

DEFINITION OF TERMS

SNR: Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power. For this data sheet noise is considered to be the power from all spectral components except for the fundamental signal, the first harmonic, and the second harmonic.

SFDR: Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.



PX1500-4 DATA FLOW

PX1500-4 SPECIFICATIONS AND ORDERING INFORMATION

External Signal Connections

Analog Inputs (4)	: SMA
Clock Input	: SMA
Trigger Input	: SMA
Sync Input	: SMA
Digital Input / Output	: SMA

Analog Inputs – Amplifier

Full Scale Voltage	: 500 mV
Impedance	: 50 ohms
Bandwidth	: dc – 1.0 GHz
SNR (dc-500 MHz)	: 46 dB
SFDR (1-500 MHz)	: 55 dB

Analog Inputs - Transformer

Full Scale Input Voltage	: 700 mV
Impedance	: 50 ohms
Bandwidth	: 5 - 2000 MHz
SNR (dc-500 MHz)	: 46 dB
(@ 1000 MHz)	: 44 dB
(@ 1500 MHz)	: 42 dB
SFDR (5-1000 MHz)	: 55 dB
(@ 1500 MHz)	: 48 dB

External Trigger

Signal Type	: LVPECL (3.3V Logic)
Impedance	: 50 ohms to +1.3V

Internal Synthesized Clock

Frequency range	: 200-1500 MHz
Resolution	: better than 62.5 PPM
Accuracy	: better than 5 PPM

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance	: 50 ohms
Termination	: Ground or +1.3V
Frequency	: 200-1500 MHz
Amplitude	: 800 mV (-300/+1200)

Post ADC Clock Divider

Divider Settings	: 1, 2, 4, 8, 16, 32
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Reference Clock

Internal	: 10.0 MHz, ± 5 ppm max.
External	: 10.0 MHz, ± 50 ppm max (required for lock)

Digitizer

Type	: ADC08D1520 (National)
Resolution	: 8 Bits
Clock Rate	: 200 – 1500 MHz

Digital Input / Output

Type	: TTL Logic Level (standard)
Max. Frequency	: 200 MHz
Connection	: series 100 ohms to FPGA I/O

Trigger Modes

Post Trigger	: single start trigger fills active memory
Pretrigger	: single trigger stops acquisition
Segmented	: start trigger for each memory segment

Trigger Options

Pretrigger Samples	: 8k samples max., total all channels
Delayed Trigger	: 64k digitizer clock cycles max.

Memory

Total Size	: 2 Gigasamples
Segment Size	: Up to 128 Megasamples
Segment re-arm time ¹	: 150 nanoseconds
Addressing	: DMA transfer from starting address

Signatec Auxiliary Bus (Version 4)

Data Transfer Rates	: TBD
Data Direction	: output only

Power Requirements

+12V	: 1.0 Amps max.
+3.3V	: 3.3 Amps max.

Absolute Maximum Ratings

Analog Inputs	: ± 3.5 volts
Trigger Input	: -0.2 to +4.0 volts DC
Clock Input	: 5 volts peak to peak
Ambient Temperature	: 0 to 50 C

Part Numbers

The PX1500-4 has the following part number modifiers that determine the configuration of the board. These are as follows:

-AMP	: Amplifier Connected Front End
-XF	: Transformer connected Front End
-SP95	: V5 SX95T Sized User Programmable FPGA
-MS	: Configured for Master/Slave Operation

The PX1500-4 part number nomenclature is as follows:

[Board Name]-[opt SP]-[AMP or XF]-[opt MS]

Example: **PX1500-4-SP95-AMP-MS** would call for a PX1500-4 board with the Virtex 5 SX95T sized user programmable FPGA, the amplifier signal input path, and master/slave configuration. The signal processing SP and master/slave modifiers are not required and should only be included when these options are exercised.

SAB Cables

Refer to the “SAB Cable Assembly Ordering Guide” to select and order the appropriate cable assemblies if required.

Master-Slave Cables

The PX1500-4 may be software configured to operate as a Master or a Slave in a multiple board system. For Master/Slave operation a 26-conductor ribbon cable is required to connect the boards. To specify master/slave configuration, order part number with ending of **-MS**. Master/Slave boards must occupy adjacent slots. The maximum number of boards to be connected is one master and two slaves. Synchronized systems with up to 6 PX1500-4 boards can be mechanized by utilizing Signatec’s Synch1500-6 clock and trigger synchronization card, which also allows for the different PX1500-4 boards to span across multiple computer chassis, if needed.

Documentation & Accessories

The PX1500-4 is supplied with a comprehensive operator’s manual, which thoroughly describes the operation of both the hardware and the software. Also supplied are four four-foot coaxial cables with SMA to BNC connectors. Additional cables may be purchased. Supplied software disks contain a function library for Microsoft Visual C/C++, example programs, and all source code to examples.

Product Warranty

All Signatec products carry a full 1-year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. This warranty does not cover customer misuse or abuse of the products or physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

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