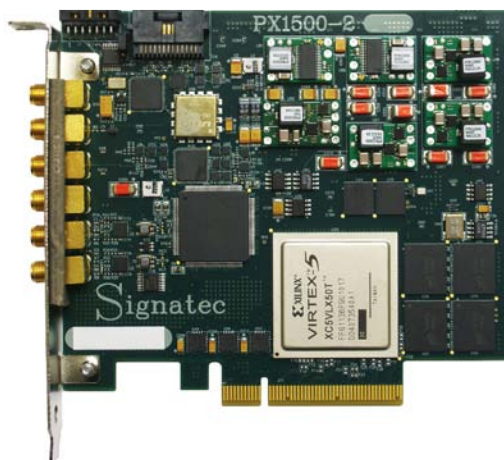


**FEATURES**

- 2 Analog Channels at up to 1500 MHz Sample Rate per Channel
- 1 Analog Channel at up to 3000 MHz Sample Rate in Interleaved Mode
- 8 Bits of Resolution
- Bandwidth up to 2 GHz
- 1 Gigabyte of On-Board Memory
- 1400 MB/s Continuous Transfer over PCI Express Bus (8 lanes)
- Tunable ADC Clock to Any Frequency from 200 MHz to 3000 MHz (effectively)
- Continuous Recording Capability Direct to PC with no Lost Samples
- Segment, Pre-trigger Samples, Post-trigger Samples and Time Stamp Capabilities
- External Trigger and External ADC Clock Inputs

APPLICATIONS

- SIGINT
- RADAR
- LIDAR
- Spectroscopy
- Mass Spectrometry – Time of Flight
- RF Communications
- Ultrasound
 - Medical Diagnostics
 - Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed / High Resolution Waveform Capture

OVERVIEW

The PX1500-2 is a two channel waveform capture board that can acquire up to 1500 mega-samples per second (MSPS) on each channel or up to 3000 MSPS for single channel operation when ADC data is interleaved. The PX1500-2 can be set up to use either a transformer coupled front end or an amplifier connection. The transformer connection can only be set for AC coupled operation and has a frequency capture range of 5 MHz to 2 GHz. The amplifier can be set for either AC or DC coupled operation with a frequency range of up to 1 GHz.

The board features an 8 lane PCI Express connection to the computer host as well as 1 gigabyte (GB) of on-board memory. If the average acquisition data rate does not exceed 1400 megabytes per second (MB/s) then the entire 1 GB memory may be used as an exceptionally large FIFO for acquiring non-stop, continuous data directly to the PCI Express bus. Significant test data has shown that recording with large FIFO buffering can be continuous at these rates even when operating in traditional non real-time environments such as the Windows operating system.

The PX1500-2 is designed to be a high performance wideband signal recording card that is economically priced. To achieve economic advantages, onboard FPGA data processing is not available on this -2 version of the PX1500 product line. If FPGA processing is required, please refer to the PX1500-4 product data sheet.

The PX1500-2 was designed to maximize the quality of the captured signal in terms of signal-to-noise ratio and spurious-free dynamic range over a very wide frequency range.

A frequency synthesized clock allows the ADC sampling rate to be set to virtually any value from 200 MHz, the minimum allowable ADC clock, to 1500 MHz, offering maximum flexibility for sampling rate selection. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, 5 PPM reference clock or to an externally provided 10 MHz reference clock. The ADC may also be clocked from an external clock source.

Digitizing at frequencies in excess of 1500 MHz involves the on-chip ADC interleave feature. When data interleaving is activated, the ADC input clock is $\frac{1}{2}$ the sampling frequency.

Up to three PX1500-2 boards may be interconnected in a Master/Slave configuration via a ribbon cable that connects at the top of the board. In this configuration the clock and trigger signals from the Master drive the Slave boards so that data sampling on all boards occurs simultaneously. Up to six boards can be set up for fully synchronized operation by utilizing the SYNC1500-6 as the clock and trigger source for the system. Users are likely better served to use the PX1500-4 for higher channel count based applications.

HARDWARE DESCRIPTION

Analog Input Section

The analog input circuitry for the 2 channels is identical, where the 2 input channels are labeled as Channel 1 and Channel 2. The board can be set up to use either a transformer coupled front end or an amplifier connection. The transformer input allows for higher frequency operation, up to 2 GHz, as well as slightly better performance in terms of SNR and SFDR. The amplifier provides the ability to capture lower frequencies and operate at lower signal levels.

Data Flow

The block diagram on page 4 shows how the data flows through the system. In normal operation, data flows through the various circuit functions via a series of self-managed FIFO to FIFO transfers.

Operating Modes

The PX1500-2 has 4 operating modes as follows:

1. Standby – the only passive mode with no data activity.
2. RAM Acquisition – waveform data is captured into the on-board RAM.
3. PCIe Buffered Acquisition – waveform data is passed to the PCIe bus, using the on-board RAM as a very large FIFO.
4. PCIe Transfer – transfer data to the PCIe bus after a RAM Acquisition.

Of particular interest is the PCIe buffered acquisition mode, where the SDRAM is operated as a large FIFO for acquiring data directly to the host system memory via the PCI Express bus. A large FIFO is necessary when acquiring large amounts of data to the PCIe bus in order to prevent data loss due to the host system's intermittent PCIe bus activity.

Triggering

The external trigger input can be used to synchronize the start of data acquisition with an external event. In order to support precise, high speed triggering, this signal is a LVPECL input that is terminated with 50 ohms to +1.3 volts. This is the proper termination for a LVPECL signal source based on +3.3V VCC. The trigger occurs on the positive going edge.

Precise, synchronized triggering of multiple PX1500-2 boards can be obtained by connecting up to three boards in a master/slave connection whereby the master board provides the trigger, clock, and sync signals for one or two slave boards. The master/slave connection is made via a ribbon cable across the top of the boards.

Up to six PX1500-2 boards can be operated in synchronization when driven by the SYNC1500-6 Clock and Trigger board. This provides the very precise clock, trigger, and sync signals for all six boards.

Acquisition may also be set to occur based on the amplitude level of the signal on input Channel 1. Both a high level and a low level threshold may be set up. The triggering thresholds are digital values that are compared against the digitized signal. Triggering can be set to occur when the signal exceeds either the high level or low level threshold.

Trigger Modes and Options

In data acquisition mode, two triggering modes are available: single shot or segmented. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. The PCIe buffered acquisition mode can be combined with the segmented trigger mode for creating high-speed continuous segment recordings.

Time Stamps

In Segmented Mode “time stamps” allow for storing the time relationship between the memory segments. Time Stamps are 64 bit timer values with a clock resolution of $4/f_{ADC}$, and are accumulated in a 2048 element FIFO memory separate from the data. If necessary, time stamps may be read during acquisition in order to prevent overflow. This is possible in any acquisition mode.

Samples Settings

There are several board settings that affect the quantity and method of acquiring samples.

Active Memory Size – This is the number of samples that will be taken after which the memory will be considered “full” and the acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt. The amount of memory that is activated for data acquisition is programmable up to 1 GB in steps of 16 bytes. In buffered acquisition modes it is also possible to operate in a “free run” mode whereby data is collected until the board is commanded to terminate the acquisition.

Segment Size – In Segmented Mode this is the number of samples that will be taken each time a valid trigger signal is detected.

Pretrigger Samples – This is the number of samples that will be recorded into RAM that occurred before the trigger.

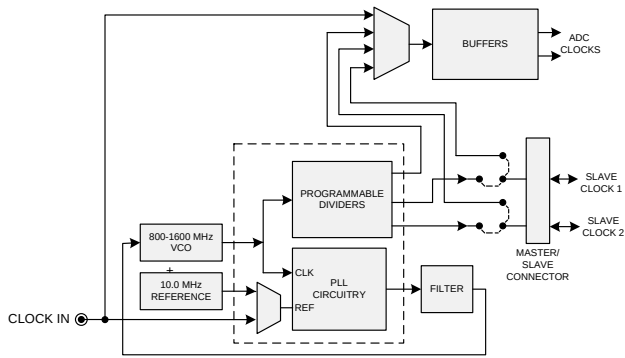
Delayed Trigger – This sets a delay between the actual applied trigger and the effective trigger for the board. The delay range is from 0 to 64k digitizer clock cycles. In Pretrigger Samples mode the delayed trigger setting establishes the number of post-trigger samples that will be recorded.

HARDWARE DESCRIPTION (CONTINUED)

ADC Clock Circuit

A functional pictorial for the PX1500-2 clock circuitry is shown in the figure below. The ADC clocks can be selected from one of four sources; an external clock, an internal synthesized clock, or 1 of the 2 slave clock inputs.

The internal synthesized clock is the primary clock source for the ADCs. The synthesized clock can generate any clock frequency from 200 to 1500 MHz to a resolution of 62 ppm or better.



For all clock sources the effective digitization rate can be further reduced via sample discarding of the digitized data. This second divider, located inside the System FPGA, can be set from 2 to 32 in factors of 2.

The synthesizer clock is locked to a 10 MHz reference clock. The reference clock may be selected from the internal reference or an externally supplied 10 MHz reference clock. The internal reference clock is accurate to better than 5ppm. This sets the ADC clock accuracy to also be within 5ppm.

Interleaved Clocking

The PX1500-2 can be set to perform interleaved clocking. In this mode the signal from one of the ADC inputs is sampled by both ADCs in the same package, but on the opposite edges of the sampling clock. In this mode the sample rate can be as high as 3.0 GHz. This allows for capturing a full 1500 MHz of bandwidth. The number of input channels is reduced from two to one in this mode; in which only Channel 1 can be the active channel for interleaved mode.

Sync Input

A sync signal is required to synchronize the ADCs on multiple PX1500-2 boards. If two or three boards are connected in a master/slave group, the sync signal is provided by the master board over the master/slave cable. If more than three boards are to be synchronized, the external clock and trigger board (SYNC1500-6) should be used. It will provide clock, trigger, and sync signals over coaxial cables via the PX1500-2 SMA connectors.

SAB Operation

The PX1500-2 does not support the Signatec Auxiliary Bus (SAB). If the SAB is required, users should use the PX1500-4 version card, which does support the SAB.

PCI Express Operation

The PX1500-2 is capable of sustaining a long-term data-transfer rate, over the PCIe bus, up to 1400 megabytes per second. If the average input data rate does not exceed this rate then PCI Buffered Acquisition mode can be utilized to stream long-term, uninterrupted data flow to the PC. The average input data rate can be reduced via any combination of the following:

1. Reducing the ADC sample rate;
2. Using fewer input data channels;
3. Using Segmented Data Acquisition.

Very-high-speed RAID systems are available that can store data indefinitely at a 1400 MB/s rate.

Signal Processing

The PX1500-2 does not support onboard FPGA data processing. If real-time data processing is required, the PX1500-4-SP95 version of the PX1500 product line supports FPGA processing. Please refer to the PX1500-4 data sheet and materials for more information.

Software

The PX1500-2 is supplied with the following software:

- Windows 32-bit & 64-bit drivers
- Linux 32-bit & 64-bit drivers (Available in Q4 2010)
- C/C++ Callable Function Library
- Turnkey signal recording software application
- Software manual that describes the PX1500-2 and information for using the available library of functions or API
- SDK offering multiple coding examples for PC side applications

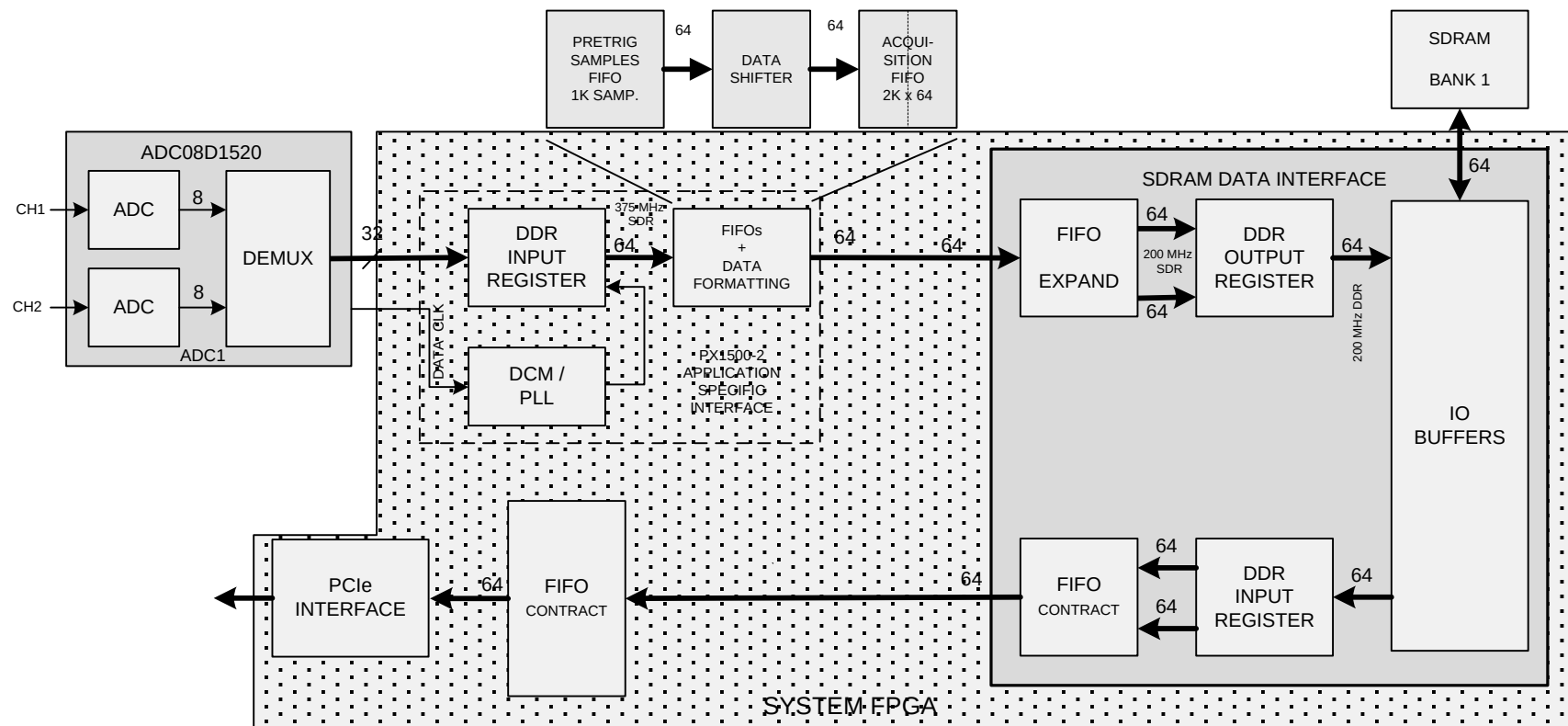
The PX1500-2 has the following optional software/firmware packages:

- LabVIEW driver, VIs, software development kit and manual

DEFINITION OF TERMS

SNR: Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power. For this data sheet noise is considered to be the power from all spectral components except for the fundamental signal, the first harmonic, and the second harmonic.

SFDR: Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.



PX1500-2 DATA FLOW

PX1500-2 SPECIFICATIONS

External Signal Connections

Analog Inputs (2)	: SMA
Clock Input	: SMA
Trigger Input	: SMA
Sync Input	: SMA
Digital Input / Output	: SMA

Analog Inputs – Amplifier

Full Scale Voltage	: 500 mV
Impedance	: 50 ohms
Bandwidth	: dc – 1.0 GHz
SNR (dc-500 MHz)	: 42 dB
SFDR (1-500 MHz)	: 53 dB

Analog Inputs – Transformer

Full Scale Input Voltage	: 700 mV
Impedance	: 50 ohms
Bandwidth	: 5 - 2000 MHz
SNR (dc-500 MHz)	: 44 dB
(@ 1000 MHz)	: 42 dB
(@ 1500 MHz)	: 40 dB
SFDR (5-1000 MHz)	: 55 dB
(@ 1500 MHz)	: 48 dB

External Trigger

Signal Type	: LVPECL (3.3V Logic)
Impedance	: 50 ohms to +1.3V

Internal Synthesized Clock

Frequency Range	: 200-1500 MHz
Resolution	: better than 62.5 PPM
Accuracy	: better than 5 PPM

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance	: 50 ohms
Termination	: Ground or +1.3V
Frequency	: 200-1500 MHz
Amplitude	: 800 mV (-300/+1200)

Post ADC Clock Divider

Divider Settings	: 1, 2, 4, 8, 16, 32
------------------	----------------------

Reference Clock

Internal	: 10.0 MHz, ± 5 ppm max.
External	: 10.0 MHz, ± 50 ppm max (required for lock)

Digitizer

Type	: ADC08D1520 (National)
Resolution	: 8 Bits
Clock Rate	: 200 – 1500 MHz

Digital Input / Output

Type	: TTL Logic Level (standard)
Max. Frequency	: 200 MHz
Connection	: series 100 ohms to FPGA I/O

Trigger Modes

Post Trigger	: single start trigger fills active memory
Pretrigger	: single trigger stops acquisition
Segmented	: start trigger for each memory segment

Trigger Options

Pretrigger Samples	: 8k samples max., total all channels
Delayed Trigger	: 64k digitizer clock cycles max.

Memory

Total Size	: 1 GB
Segment Size	: Up to 512 Megasamples
Segment Re-arm Time	: 150 nanoseconds
Addressing	: DMA transfer from starting address

Power Requirements

+12V	: 1.0 Amps max.
+3.3V	: 3.3 Amps max.

Absolute Maximum Ratings

Analog Inputs	: ± 3.5 volts
Trigger Input	: -0.2 to +4.0 volts DC
Clock Input	: 5 volts peak to peak
Operating Temperature	: +32°F to +122°F 0°C to 50°C
Storage Temperature	: -4°F to +158°F -20°C to +70°C
Operating Relative Humidity	: 10% to 90%, non-condensing
Operating Vibration	: 0.25 G, 5 Hz to 500 Hz
Operating Shock	: 2.5 G, 11 ms, ½ sine
Board Dimensions	: 5" L x 4.3" H x 0.75" W 12.7cm L x 10.9cm H x 1.9cm W

PX1500-2 ORDERING INFORMATION

Part Number Ordering Information

The PX1500-2 part number nomenclature for ordering is as follows:

PX1500-2-[Coupling]-[Front End Path]-[Master/Slave]

[Coupling]:

- A** : AC Coupled for All Channels
- D** : DC Coupled for All Channels
- AD** : AC Coupled Channel 1 / DC Coupled Channel 2
- DA** : DC Coupled Channel 1 / AC Coupled Channel 2

[Front End Path]:

- A** : Amplifier Connected Front End for All Channels with Frequency Capture Range up to 1GHz and Support for DC Offset Adjustment.
- X** : Transformer Connected Front End for All Channels with Frequency Capture Range of 5MHz to 2GHz and Fixed DC Offset. This option requires [Coupling] selection to be specified as "A".
- AX** : Amplifier Connected Front End for Channel 1 with Frequency Capture Range up to 1GHz and Support for DC Offset Adjustment / Transformer Connected Front End for Channel 2 with Frequency Capture Range of 5MHz to 2GHz and Fixed DC Offset. This option requires [Coupling] selection to be specified as either "A" or "DA".
- XA** : Transformer Connected Front End for Channel 1 with Frequency Capture Range of 5MHz to 2GHz and Fixed DC Offset / Amplifier Connected Front End for Channel 2 with Frequency Capture Range up to 1GHz and Support for DC Offset Adjustment. This option requires [Coupling] selection to be specified as either "A" or "AD".

[Master/Slave]: This is optional. Do not specify unless required.

- MS** : Configured for Master/Slave Cable Operation
- SY** : Configured for Master/Slave Operation with SYNC1500

The master/slave modifiers "**MS**" or "**SY**" are not required for standalone operation of individual boards, and should only be included in the ordering part number when planning to use multiple boards together for synchronized multi-board channel operations.

The PX1500 is hardware configured to operate as a Master or a Slave in a multiple board system. Designated Slave modified boards can not operate independently as standalone boards.

With the specified "**MS**" part designator, a 26-pin conductor ribbon cable is required and supplied to connect the boards together. Master/Slave "**MS**" boards must occupy adjacent slots. The maximum number of "**MS**" boards that can be connected is three: one master board and two slave boards.

With the specified "**SY**" part designator, boards are configured to operate with Signatec's SYNC1500-6 (sold separately) clock and trigger synchronization card. Synchronized systems with up to six PX1500-2 boards can be mechanized with the SYNC1500-6, which also allows for the different PX1500-2 boards to span across multiple computer chassis if needed. For high channel count applications, the alternative PX1500-4 product option should be considered as it provides a better cost per channel average.

Part Number Order Examples

The following are some valid part number ordering examples (this list does not depict all possible combinations):

- PX1500-2-A-A** : PX1500-2 with AC based coupling for both channels and amplifier connected front end for both channels.
- PX1500-2-A-X** : PX1500-2 with AC based coupling for both channels and transformer connected front end for both channels.
- PX1500-2-D-A** : PX1500-2 with DC based coupling for both channels and amplifier connected front end with both channels.
- PX1500-2-A-AX** : PX1500-2 with AC based coupling for both channels and amplifier connected front end for Channel 1 and transformer connected front end for Channel 2.
- PX1500-2-DA-AX** : PX1500-2 with DC based coupling and amplifier front end for Channel 1, and AC AC based coupling and transformer connected front end for Channel 2.
- PX1500-2-A-A-MS** : PX1500-2 with AC based coupling for both channels and amplifier connected front end with both channels, and configured for Master/Slave based cable operation.
- PX1500-2-A-A-SY** : PX1500-2 with AC based coupling for both channels and amplifier connected front end with both channels, and configured for Master/Slave based SYNC1500 operation.

Documentation & Accessories

The PX1500-2 is supplied with a comprehensive operator's manual, which thoroughly describes the operation of both the hardware and the software. Also supplied are four four-foot coaxial cables with SMA to BNC connectors. Additional cables may be purchased. Supplied software disks contain a function library for Microsoft Visual C/C++, example programs, and all source code to examples.

Product Warranty

All Signatec products carry a standard full 1-year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer.

Optional Extended Warranty Plans are also available for purchase for up to a maximum 5-year warranty period.

Standard and Optional Extended Warranties do not cover customer misuse or abuse of the products or physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

Data Sheet Revision 1.01 – 09/10/2010