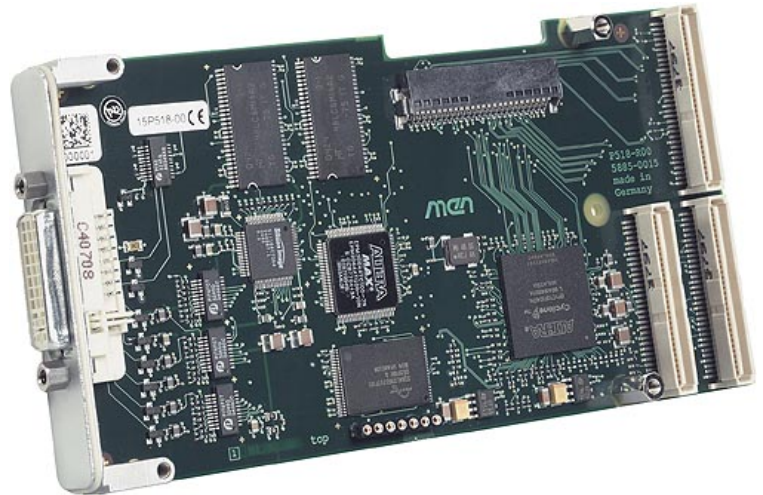


P518 – Frame Buffer Interface PMC

- **Frame buffer functionality in FPGA**
- **FPGA 12,000 LEs (approx. 144,000 gates)**
- **Color depth 16-bit RGB**
- **640 x 480 up to 1280 x 1024 pixels resolution**
- **Frequencies 60 Hz and 75 Hz**
- **32 MB integrated graphics RAM**
- **DVI digital video output (DVI-I front connector)**
- **LVDS TFT via rear-I/O or on-board connector**
- **-40 to +85°C with qualified components**



The P518 comes with frame buffer functionality and is typically used as an extension card for PCI-based systems. The complete set of graphics instructions is realized inside an FPGA, with the FPGA acting as a PCI target (32-bit/33-MHz or 32-bit/66-MHz). Using FPGA technology to implement graphics in a system provides the advantage of nearly unlimited availability - which is ideal for industrial applications. And since the FPGA is available in -40 to +85°C operation temperature from the chip manufacturer, the complete P518 module is delivered in this extended temperature range. The P518 is equipped with a DVI digital video output connector. An LVDS TFT interface is accessible via the

on-board connector or the rear-I/O connector. A 32-MB, 133-MHz SDRAM is implemented as a local frame buffer. Its data bus width is 32 bits.

Multiple display modes are configurable by updating a configuration Flash. The graphics controller itself will be loaded with the new Flash data via a small configuration PLD after restart.

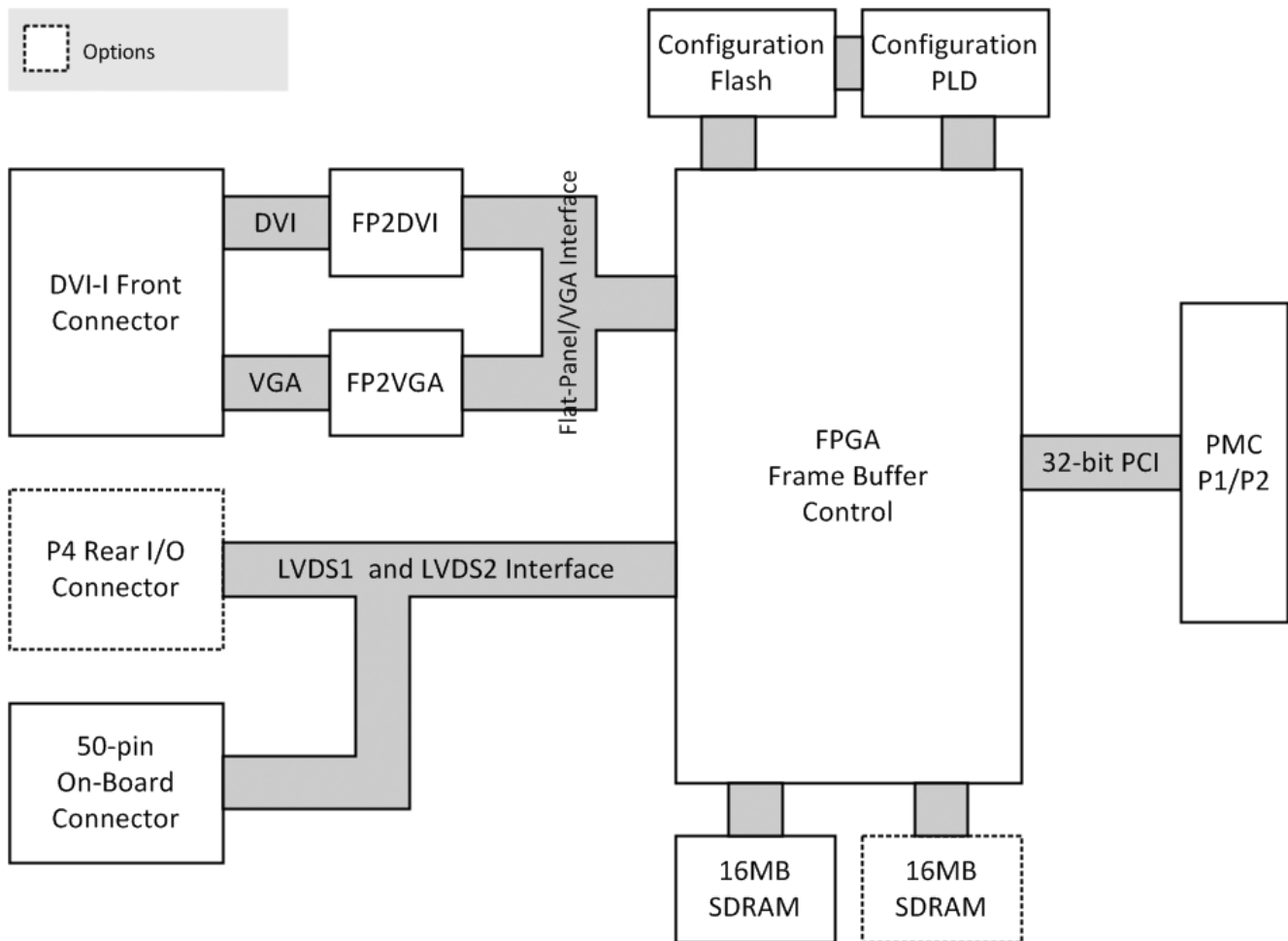
The graphics controller video outputs are flat panel signals. Conversion to both VGA and DVI is done by separate hardware.

The graphics clock is supplied directly by a 48-MHz oscillator.

The same functionality is also available on PC-MIP®, a PCI-based mezzanine card in a smaller form factor.

The P518 is a PMC I/O mezzanine card suitable for any PMC compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC. Appropriate PMC carrier cards in 3U, 6U and other formats are available from MEN or other manufacturers.

Diagram



Technical Data

Video Signals	■ DVI interface; FP to DVI conversion ■ VGA interface; FP to VGA conversion ■ LVDS TFT interface via on-board connector or optional rear I/O connector ■ Color depth 16-bit RGB ■ Resolutions DVI/VGA (change only by FPGA update) □ 640x480 □ 800x600 □ 1024x768 □ 1280x1024 ■ Resolutions LVDS (change only by FPGA update) □ 640x480, 800x600 or 1024x768 with one or two LVDS connections □ 1280x1024 with two LVDS connections only ■ Frequencies: DVI/VGA 60 Hz or 75 Hz; LVDS 60 Hz
Memory	■ 32 MB/133 MHz SDRAM with 32-bit memory interface
FPGA	■ Standard FPGA graphics configuration □ Main bus interface □ 16Z044_DISP - Display controller □ 16Z043_SDRAM - SDRAM controller □ 16Z045_FLASH - Flash interface ■ The FPGA offers the possibility to add customized I/O functionality. See FPGA. ■ Examples of graphics extensions: □ Video compression □ Bit blitter □ Rendering □ Pattern recognition □ ...
Peripheral Connection	■ Flat-panel and VGA signals via DVI-I front connector ■ LVDS signals via P1 onboard connector
PMC Characteristics (PCI)	■ Compliant with PCI Specification 2.2 ■ 32-bit/33-MHz, 3.3V V(I/O); 66 MHz on request ■ Target
Electrical Specifications	■ Supply voltage/power consumption: □ +5V (4.85..5.25V), 10 mA max. □ +3.3V (3.0..3.6V), 300 mA typ.
Mechanical Specifications	■ Dimensions: conforming to IEEE 1386.1 ■ Weight: 70 g
Environmental Specifications	■ Temperature range (operation): □ -40..+85°C □ Airflow: min. 10 m³/h ■ Temperature range (storage): -40..+85°C ■ Relative humidity (operation): max. 95% non-condensing ■ Relative humidity (storage): max. 95% non-condensing ■ Altitude: -300 m to + 3,000 m ■ Shock: 15 g/11 ms ■ Bump: 10 g/16 ms ■ Vibration (sinusoidal): 2 g/10..150 Hz ■ Conformal coating on request
MTBF	■ MTBF: 426,000 h @ 40°C (derived from MIL-HDBK-217F)
Safety	■ PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers
EMC	■ Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Technical Data

Software Support

- Windows®
- Linux
- VxWorks® (WindML)
- QNX®
- [For more information on supported operating system versions and drivers see Downloads.](#)

FPGA

This product offers the possibility to add customized I/O functionality in FPGA.

Flexible Configuration

- Customized I/O functions can be added to the FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- [You can find more information on our web page "User I/O in FPGA"](#)

FPGA Capabilities

- FPGA Altera® Cyclone® EP1C12
 - 12,060 logic elements
 - 239,616 total RAM bits
- Configuration data stored in 2MB Flash
- MEN offers Flash update tools for different operating systems.

Configuration & Options

Standard Configurations

Article No.	Resolution	SGRAM	Operation Temperature
15P518-00	800 x 600	32 MB	-40..+85°C

Options

Peripheral Connection	■ LVDS signals via P4 rear I/O connector
Resolution	■ 640x480 ■ 800x600 ■ 1024x768 ■ 1280x1024 (two LVDS connections needed for LVDS support!)
SGRAM	■ 16 MB or 32 MB
Operation Temperature	■ -40..+85°C

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

Ordering Information

Standard P518 Models	15P518-02	FPGA-based frame buffer interface, resolution 800x600, 32MB integrated SGRAM, without rear I/O, -40..+85°C with qualified components
Miscellaneous Accessories	05P000-01	25 mounting screw sets to fix PMC/XMC modules on carrier boards
Software: FPGA	16P018-00	P518/P18 FPGA file for frame buffer functionality (PCI, SDRAM, 18-bit TTL RGB, LVDS, Flash)
Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	13Z044-90	Linux native driver (MEN) for 16Z044_DISP (frame buffer)
	13Z100-91	Linux FPGA update tool (MEN)
Software: Windows®	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN.	
	13Z044-70	Windows® native driver (MEN) for 16Z044_DISP (frame buffer)
	13Z100-70	Windows® FPGA update tool (MEN)
Software: VxWorks®	This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z044-60	VxWorks® driver (MEN) for 16Z044_DISP (frame buffer)
	13Z100-60	VxWorks® FPGA update tool (MEN)
Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z044-40	QNX® native driver (MEN) for 16Z044_DISP (frame buffer)
	13Z100-40	QNX® FPGA update tool (MEN)
Software: Miscellaneous	XiBase9, a graphical user interface from XiSys, is running on the MEN graphics controller PMC module P518 in combination with the PowerPC®-based single-board computer A15C running OS-9®. The necessary drivers are available on request, for more information please contact our sales staff.	
For operating systems not mentioned here contact MEN sales .		
Documentation	Compare Chart mezzanine functions on PMC/XMC and PC-MIP® » Download	
	20P518-00	P518 User Manual

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