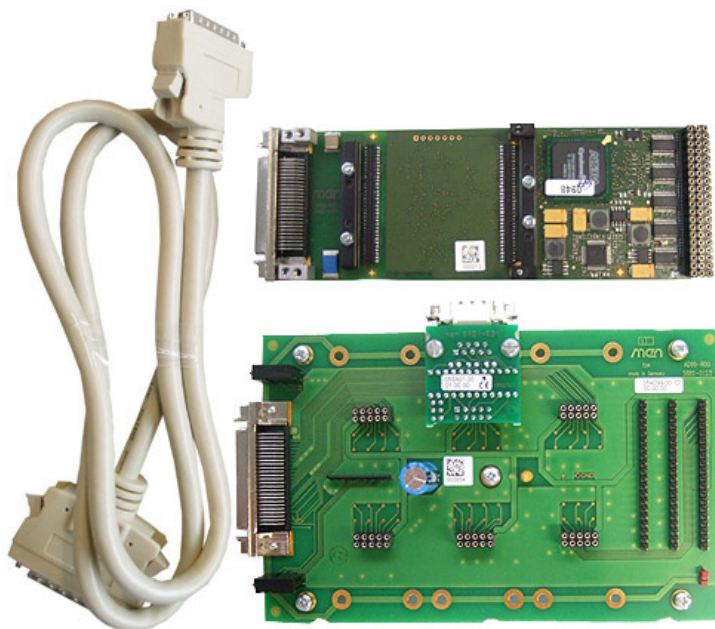


M-Module™ USM™ FPGA Development Kit

- **1 Main M-Module™ M199 for USM™ Universal Submodules:**
 - **1 FPGA 33,216 LE**
 - **32 MB DDR2 SDRAM, 8 MB Flash**
- **1 bare USM™ module US0**
- **1 evaluation board with RS232 debug interface**
- **1 FPGA development package:**
 - **Main bus interface**
 - **Memory control**
 - **Nios® soft core**
 - **Wishbone/Avalon® bridges**
 - **For user-defined I/O**
- **1 SCSI cable**
- **-40 to +85 °C with qualified components**



USM™ Universal Submodules make M-Modules™ more flexible, cost and time-saving than ever. A main M-Module™ gets its specific function through the IP cores implemented inside its onboard FPGA. This function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on a USM™ which is simply plugged on the main M-Module™.

This FPGA USM™ development kit for M-Modules™ has been prepared for users who like to write and/or implement specific IP cores on their own. Even the growing range of Wishbone-based standard IP cores from MEN (different UARTs, Ethernet, fieldbus interfaces, graphics, digital I/O etc.) can be combined with your own or third-party functions.

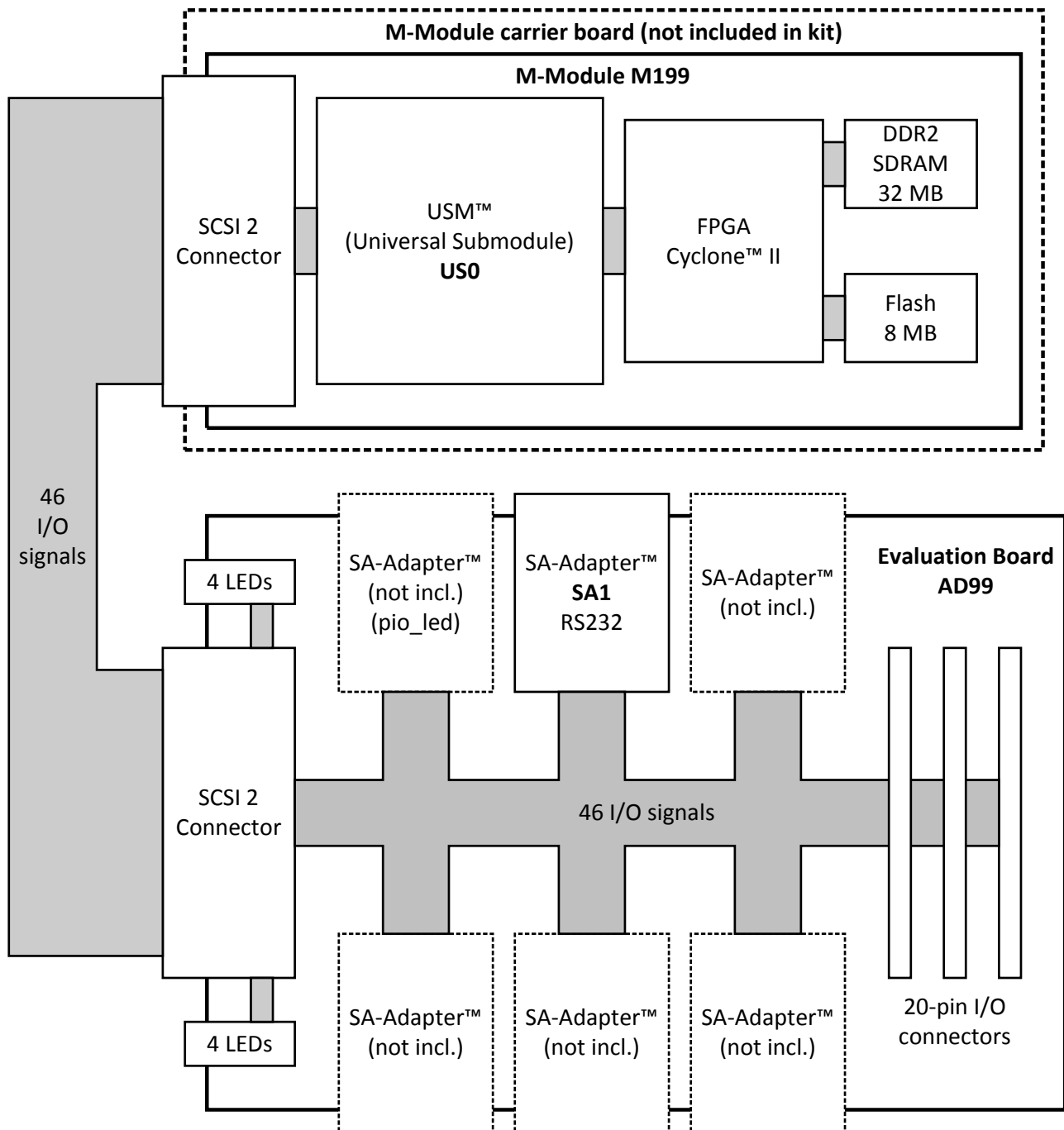
The kit includes the main M-Module™ M199 equipped with an FPGA, 32 MB DDR2 SDRAM, 8 MB Flash and a 50-pin SCSI connector. In addition the package includes a bare USM™ module, a test board where I/O signals from the FPGA are led to and where an

additional debug interface is implemented, and a SCSI cable for connection between the main M-Module™ and test board. The Nios® processor, memory control, and the Avalon®/Wishbone bridges are installed on the main module. The corresponding FPGA development package is available as web download. For development of IP cores on the standard Wishbone bus the Wishbone Bus Maker tool from MEN is included. In order to use the Nios® cores and to develop IP cores on the Avalon® bus Altera®'s Quartus® II design environment including the SOPC builder is needed separately.

ANSI standard mezzanine M-Modules™ can be used as an I/O extension in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC. Appropriate M-Module™ carrier cards in 3U, 6U and other formats are available from MEN or other manufacturers.

Once a USM™ module has been developed for M-Modules™, it may also be used on PMC or XMC and conduction-cooled PMC base modules, and vice versa.

Diagram



Technical Data

Evaluation Board AD99	■ 50-pin connection to M199 □ SCSI 2 connector □ 46 I/O signals from/to M199 ■ Six SA-Adapter™ slots □ For direct onboard connection □ 46 I/O signals from/to SCSI 2 connector □ RS232 SA-Adapter™ SA1 included ■ Three 20-pin I/O connectors □ 46 I/O signals from/to SCSI 2 connector ■ Eight user LEDs at front, driven by I/O signals
M-Module™ M199 (USM™ main module)	■ CPU □ Nios® II soft processor □ 66MHz ■ Memory □ 32MB DDR2 SDRAM, soldered □ 8MB non-volatile Flash, for FPGA data and Nios® firmware ■ I/O at front panel (SCSI 2 connector) □ One LVTTTL UART (for RS232 on AD99 via SA1 SA-Adapter™) ■ Functions in FPGA □ Main bus interface □ Altera® SOPC Unit incl. Nios® II/f soft processor, GPIO, UART and DDR2 SDRAM control □ Wishbone-to-Avalon®/Avalon®-to-Wishbone bridges □ Reset controller, interrupt controller, SMBus controller, GPIO controller □ M-Module™ to Wishbone bridge, ID EEPROM emulation □ 16Z045_FLASH - Flash interface □ The FPGA offers the possibility to add customized I/O functionality. See FPGA. ■ USM™ Slot □ One slot populated with bare USM™ module US0 □ US0 only passes through signals between the FPGA and the front connector and reduces +5V input levels to 3.3V system I/O level ■ Connection to evaluation board □ SCSI 2 connector, 50-pin HP D-Sub receptacle □ 46 I/O signals from/to evaluation board, FPGA-controlled ■ M-Module™ Characteristics □ Compliant with M-Module™ standard □ A08, A24, D08, D16, D32, INTA, IDENT
Accessories	■ SA1 RS232 SA-Adapter™ ■ SCSI 2 cable ■ Please note that the kit does not include an M-Module™ carrier board! You should install the M-Module™ on a suitable carrier in a test system of your choice.
Electrical Specifications	■ Supply voltage/power consumption: □ M199 with US0: +5V (-3%/+5%), 1000mA max. □ AD99: +5V, consumption only depends on SA-Adapter™ used, current drawn on I/O lines and LEDs driven, with 1 SA1 and all 8 LEDs on approx. 100mA typ. □ SA1: +5V (-3%/+5%), 40mA typ. ■ MTBF: □ M-Module™ USM™ Development Kit (total): 319,364h @ 40°C according to IEC/TR 62380 (RDF 2000) □ M199: 533,355h @ 40°C according to IEC/TR 62380 (RDF 2000) □ US0: 1,989,261h @ 40°C according to IEC/TR 62380 (RDF 2000) □ AD99: 1,469,985h @ 40°C according to IEC/TR 62380 (RDF 2000) □ SA1: 1,870,000h @ 50°C (derived from MIL-HDBK-217F)

Technical Data

Mechanical Specifications	■ Dimensions: □ M199: conforming to M-Module™ standard □ US0: conforming to USM™ standard □ AD99: standard single Eurocard, 100mm x 160mm □ SA1: 32mm x 42mm ■ Weight: □ M199: 70g □ US0: 20g □ AD99: 90g □ SA1: 16g
Environmental Specifications	■ Temperature range (operation): □ 0..+60°C □ Airflow: min. 10m³/h ■ Temperature range (storage): -40..+85°C ■ Relative humidity (operation): max. 95% non-condensing ■ Relative humidity (storage): max. 95% non-condensing ■ Altitude: -300m to + 3,000m ■ Shock: 15g/11ms ■ Bump: 10g/16ms ■ Vibration (sinusoidal): 2g/10..150Hz ■ Conformal coating on request
Safety	■ PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers
EMC	■ Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)
Software Support	■ Nios® sample design for Quartus® II development tools ■ Flash update tools for Windows®, Linux, VxWorks® ■ Driver software depending on implemented FPGA functions ■ For more information on supported operating system versions and drivers see Downloads.

FPGA

This product offers the possibility to add customized I/O functionality in FPGA.

Flexible Configuration	■ Customized I/O functions can be added to the FPGA. ■ It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility. ■ You can find more information on our web page "User I/O in FPGA"
FPGA Capabilities	■ FPGA Altera® Cyclone® II EP2C35 □ 33,216 logic elements □ 483,840 total RAM bits ■ Connection □ Functions can be linked to Wishbone or Avalon® bus □ Available pin count: 46 pins (FPGA to USM™) □ Functions available via USM™ at front I/O connector of M199 and onboard connectors of AD99 evaluation board □ SA-Adapters™ can be used on AD99 to realize the physical lines. ■ MEN offers an FPGA Development Package as well as Flash update tools for different operating systems.
MEN IP Cores	■ MEN offers a large number of standard IP cores. ■ Examples: □ IDE (e.g. PIO mode 0, UDMA mode 5) □ UARTs □ CAN bus □ Display control □ Fast Ethernet (10/100Base-T) □ ... ■ For IP cores developed by MEN please refer to our IP core overview. □ IP Core compare chart (PDF) ■ MEN also offers development of new (customized) IP cores.
Third-Party IP Cores	■ Third-party IP cores can also be used in combination with MEN IP cores. ■ Examples: □ www.altera.com □ www.opencores.org
FPGA Design Environment	■ Altera® offers free download of Quartus® II Web Edition □ Complete environment for FPGA and CPLD design □ Includes schematic- and text-based design entry □ Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software □ SOPC Builder system generation software □ Place-and-route, verification, and programming ■ Altera® Quartus® II Web Edition FPGA design tool

Ordering Information

Standard M-Module™ USM™ FPGA Development Kit Models	19M199-00	M-Module™ USM™ FPGA development kit consisting of 1 FPGA-based universal M-Module™ M199, 1 bare USM™ Universal Submodule US0, 1 eval board AD99 for USM™/FPGA development, 1 SA-Adapter™ SA1 (RS232), connection cable, FPGA/Nios® example project including M-Module™ core (key for download), 0..+60°C
Related Hardware	04M199-00	USM™ main M-Module™, -40..85°C with qualified components
SA-Adapters™	If you have implemented the corresponding IP core in the FPGA, you may be able to use the following SA-Adapters™ as a physical layer on your USM™ evaluation kit:	
	08SA01-00	RS232, not optically isolated, 0..+60°C
	08SA02-00	RS422/485, half duplex, optically isolated, 0..+60°C
	08SA02-01	RS422/485, full duplex, optically isolated, 0..+60°C
	08SA03-00	RS232, optically isolated, 0..+60°C
	08SA08-00	CAN ISO high-speed, optically isolated, 0..+60°C
	08SA15-00	8 binary I/O channels, -40..+85°C with qualified components, no RoHS
	08SA22-00	IBIS master SA-Adapter™, -40..+85°C screened
	08SA22-01	IBIS slave SA-Adapter™, -40..+85°C screened
	08SA25-00	GPS receiver, isolated, -40..+85°C screened
	08SA26-00	RS422 with 15-pin D-Sub connector, with handshake signals (RTS, CTS, DCD, DTR), coated, -40..+85°C screened
Software: FPGA	16M199-00	Nios® M-Module™ USM™ FPGA Development Package (MEN) (without Altera® Quartus® II) (license included in M-Module™ USM™ FPGA Development Kit)
Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	13Z100-91	Linux FPGA update tool (MEN)
Software: Windows®	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN.	
	13Z100-70	Windows® FPGA update tool (MEN)
Software: VxWorks®	This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z100-60	VxWorks® FPGA update tool (MEN)
Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z100-40	QNX® FPGA update tool (MEN)
For operating systems not mentioned here contact MEN sales .		
Documentation	20M199-01	M-Module™ USM™ FPGA Development Kit User Manual
	20US00-00	USM™ Specification
	21M199-00	P599/M199 Programmer's Guide

Contact Information

Germany

MEN Mikro Elektronik GmbH
Neuwieder Straße 3-7
90411 Nuremberg
Phone +49-911-99 33 5-0
Fax +49-911-99 33 5-901

info@men.de
www.men.de

France

MEN Mikro Elektronik SA
18, rue René Cassin
ZA de la Châtelaine
74240 Gaillard
Phone +33 (0) 450-955-312
Fax +33 (0) 450-955-211

info@men-france.fr
www.men-france.fr

USA

MEN Micro, Inc.
24 North Main Street
Ambler, PA 19002
Phone (215) 542-9575
Fax (215) 542-9577

sales@menmicro.com
www.menmicro.com

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