

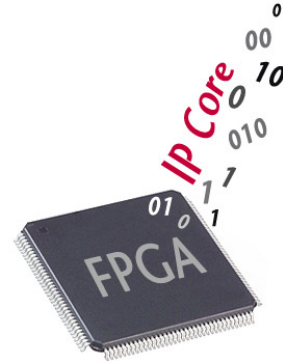
16Z034_GPIO – GPIO Controller IP Core

- **FPGA IP Core**
- **8 input/output ports**
- **Separate programmable interrupts for each input**
- **8-bit debouncer logic for input signals**
- **Outputs configurable as open drain or regular digital ports**
- **Wishbone bus interface**

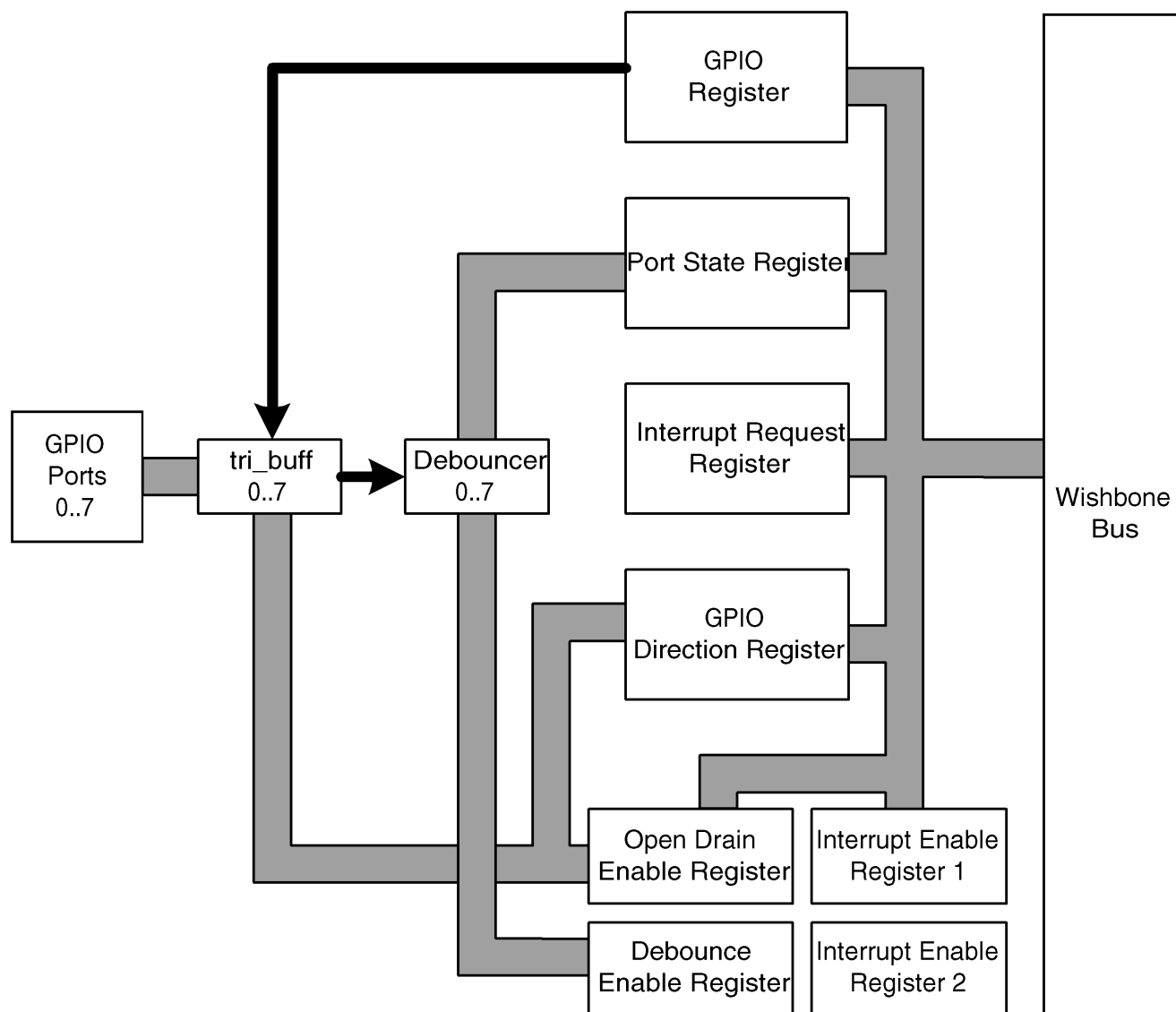
The GPIO controller is a General Purpose Input/Output module with 8 input/output ports. The module is able to generate an interrupt for each input. The usage of a pin can be set in a GPIO Direction Register. Two Interrupt Enable Registers give the possibility to set the edge of the input signal (rising, falling or both) which shall generate an interrupt. The state of the GPIO port pins can be read again and will be displayed in the Port State Register. This can be used to detect short circuits at the output pins. For general purpose input bits it is possible to include an 8-bit debouncer logic to avoid bouncing on input signals when used e.g. with a button. For general purpose output bits it is possible to

adjust whether the pin can be used as an open drain port or as a regular digital port.

MEN IP cores are described in standard VHDL language and the standard Wishbone bus is used as the system interface. By using IP cores, application-specific functions can be performed flexibly and individually in the FPGA on a growing range of MEN CPU boards. These IP cores can be assembled from the MEN function library and reconfigured, combined with IP cores from other providers or even completely redeveloped as required. The FPGA behaves just like a standard PCI component. The FPGA functions are loaded by software when the system is booted and are available in less than 1 s. On PowerPC® platforms the FPGA can be dynamically updated during operation. On Pentium® platforms FPGA updates are also possible in the boot Flash during operation and are then available once the system is rebooted.



Diagram



Technical Data

Size	■ Logic elements (Altera® Cyclone® device family): max. 250 (depending on usage of debouncer inputs) ■ Pin count min: 1 ■ Pin count max: 8
System-Bus Interface	■ Wishbone bus interface compliant with Wishbone Specification B.3 ■ 8-bit data transfer, 66MHz bus frequency ■ Supported Wishbone bus cycles □ Single read/write
GPIO Functionality	■ Up to 8 general purpose input/output ports ■ Optional debouncer for inputs ■ Optional open drain functionality ■ Interrupt on input signal change (rising and/or falling edge) ■ Re-readable outputs ■ Generics for all register values
Software Support	■ MEN Driver Interface System (MDIS™ for Windows®, Linux, VxWorks®, QNX®, OS-9®) ■ For more information on supported operating system versions and drivers see Downloads.

Ordering Information

Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN. <table> <tr> <td>13Z017-06</td><td>MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</td></tr> </table>	13Z017-06	MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO
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Software: Windows®	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN. <table> <tr> <td>13Z017-70</td><td>MDIS4™/2004 / MDIS5™ Windows® driver (MEN) for 16Z034_GPIO devices</td></tr> </table>	13Z017-70	MDIS4™/2004 / MDIS5™ Windows® driver (MEN) for 16Z034_GPIO devices
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Software: VxWorks®	This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets. <table> <tr> <td>13Z017-06</td><td>MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</td></tr> </table>	13Z017-06	MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO
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Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets. <table> <tr> <td>13Z017-06</td><td>MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</td></tr> </table>	13Z017-06	MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO
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Software: OS-9®	This product is designed to work under OS-9®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets. <table> <tr> <td>13Z017-06</td><td>MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO</td></tr> </table>	13Z017-06	MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO
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For operating systems not mentioned here contact MEN sales.			
Documentation	<table> <tr> <td>22Z034-00</td><td>16Z034_GPIO Reference Manual</td></tr> </table>	22Z034-00	16Z034_GPIO Reference Manual
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