

# 16Z043\_SDRAM – SDRAM Controller IP Core

- **FPGA IP Core**
- **Supports up to 133 MHz clock frequency**
- **Single and burst transactions**
- **Wishbone bus interface**



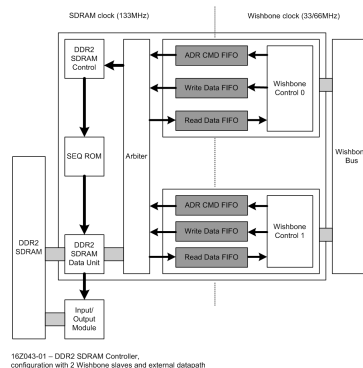
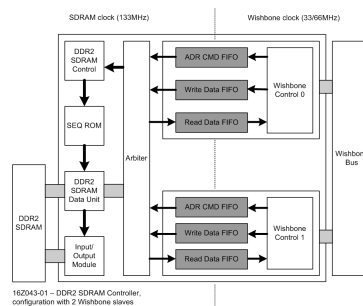
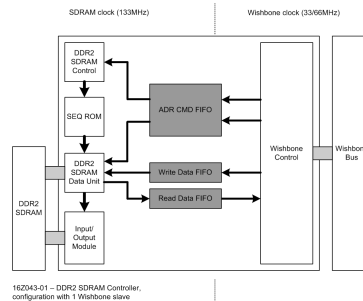
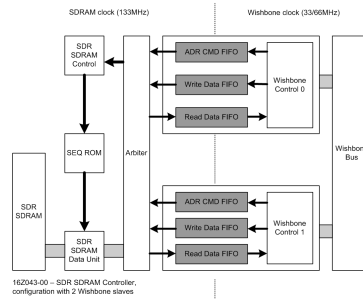
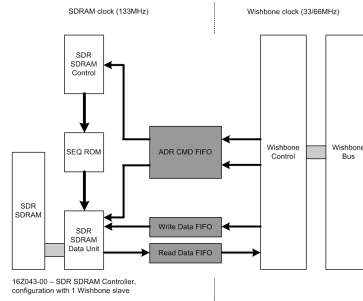
This product is an SDRAM controller for FPGA to SDRAM interfaces. The main functionality is to connect the Wishbone bus to SDRAM memory, with up to 133 MHz clock frequency. Single and burst transactions are supported. The 16Z043-00 version of this IP core is for SDR (Single Data Rate) SDRAM while the 16Z043-01 is for DDR2 (Double Data Rate 2) SDRAM.

This interface typically connects a large fast memory to a display controller in order to store graphics data.

MEN IP cores are described in standard VHDL language and the standard Wishbone bus is used as the system interface.

By using IP cores, application-specific functions can be performed flexibly and individually in the FPGA on a growing range of MEN CPU boards. These IP cores can be assembled from the MEN function library and reconfigured, combined with IP cores from other providers or even completely redeveloped as required. The FPGA behaves just like a standard PCI component. The FPGA functions are loaded by software when the system is booted and are available in less than 1 s. On PowerPC® platforms the FPGA can be dynamically updated during operation. On Pentium® platforms FPGA updates are also possible in the boot Flash during operation and are then available once the system is rebooted.

# Diagram



## Technical Data

|                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Size</b>                 | <ul style="list-style-type: none"> <li>■ Logic elements (Altera® Cyclone® device family): 1200 (16Z043-00) or ~1100 (16Z043-01)</li> <li>■ Pin count min: 38 for 16Z043-00, 43 for 16Z043-01</li> <li>■ Pin count max: 57 for 16Z043-00, 43 for 16Z043-01</li> <li>■ RAM: 5 x M4K (Cyclone® I and II) or 5 x M9K (Cyclone® III)</li> <li>■ (3 x M4K and 3 x M9K for later revisions of 16Z043-00)</li> </ul>                                              |
| <b>System-Bus Interface</b> | <ul style="list-style-type: none"> <li>■ Wishbone bus interface compliant with Wishbone Specification B.3</li> <li>■ 32-bit data transfer, up to 133MHz bus frequency</li> <li>■ Supported Wishbone bus cycles <ul style="list-style-type: none"> <li>□ Single read/write</li> <li>□ Burst read/write</li> </ul> </li> <li>■ Second Wishbone interface for enhanced data throughput</li> <li>■ Flexible FIFO depth for best system integration</li> </ul> |
| <b>SDRAM Functionality</b>  | <ul style="list-style-type: none"> <li>■ SDR SDRAM data width 16 or 32 bits (16Z043-00)</li> <li>■ DDR2 SDRAM data width 16 bits (16Z043-01)</li> <li>■ Variable CAS latency</li> <li>■ Up to 133 MHz clock rate</li> <li>■ Refresh counter</li> </ul>                                                                                                                                                                                                    |

## Ordering Information

|                      |                  |                               |
|----------------------|------------------|-------------------------------|
| <b>Documentation</b> | <b>22Z043-00</b> | 16Z043_SDRAM Reference Manual |
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