INNODISK®
Beyond your imagination

EDC 4000 Plus

Customer: _____

Customer Part Number: _____

InnoDisk Part Number: _____

InnoDisk Model Name: _____

Date: _____

InnoDisk Approver	Customer Approver

the total solution for industrial flash storage

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REVISION HISTORY

Revision	Description	Date
Rev. 1.0	First Release	Oct. 2011
Rev 2.0	Add hardware write protect function	June. 2012

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1. Introduction

Embedded Disk Card 4000 Plus (EDC4000 Plus) products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association ATA standard. InnoDisk Embedded Disk Card Plus 4000 Plus (EDC4000 Plus) is embedded solid-state data storage systems for industrial work place. Embedded Disk Card 4000 Plus (EDC4000 Plus) features an extremely light weight, reliable, low-profile form factor.

Embedded Disk Card 4000 Plus (EDC4000 Plus) supports advanced PIO (0-4), Multi Word DMA (0-2), Ultra DMA (0-4) transfer modes, multi-sector transfers, and LBA addressing.

2. Features

- The Industrial ATA products provide the following system features:
- Capacities: 128MB to 32GB
- Fully compatible with the IDE standard interface, ATA Standard
- Access modes: True IDE Mode
- ECC (Error Correction Code) function: 24 bits/ per 1024 byte
- +3.3V/+5V power supply operation
- Support Auto Stand-by and Sleep Mode.
- Power Consumption

  Active mode

  Read operation: 86mA(Typ.)

  Write operation: 140mA(Typ.)

  Power Down mode: 1mA(Typ./max.)
- Support transfer modes: PIO(0-4), Multiword DMA (0-2) and Ultra DMA(0-4)
- MTBF 3,000,000 hours

- R/W performance:

  -Single:

  - Read: 20Mbytes/s. (MAX)
  - Write: 10Mbytes/s (MAX)

  -Dual:

  - Read: 45Mbytes/s. (MAX)
  - Write: 28Mbytes/s (MAX)

- Operating temperature range: 0°C ~ +70°C(Standard Temp.)
  -40°C ~ +85°C(Industrial Temp.)
- Storage temperature range: -55°C ~ +95°C

2.1 Write Protect Function Support

EDC4000 Plus within the write-protect function could prevent the EDC from modification and deletion. Write-protected data in EDC4000 Plus could only be read, that is, users could not write to it, edit it, append data to it, or delete it.

When users would like to make sure that neither themselves nor others could modify or destroy the file, users could switch write-protection switch to “OFF” position. Thus EDC4000 Plus would process write-protect mechanism and disable flash memory to be written-in any data. Only while the system power-off, write-protection could be switched. Write-protection could not be switched after OS booting.

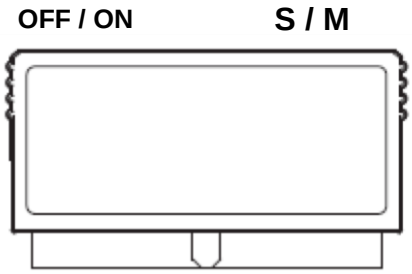

Figure 1: EDC 4000 Plus 44P Vertical type Write protect and Master/Slave switch

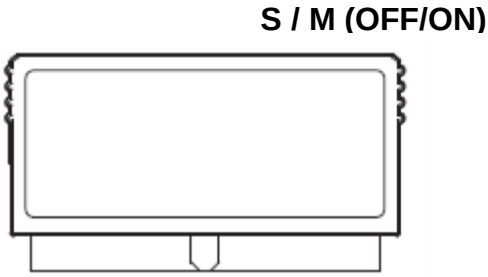

Figure 2: EDC 4000 Plus 40P Vertical type Write protect and Master/Slave switch

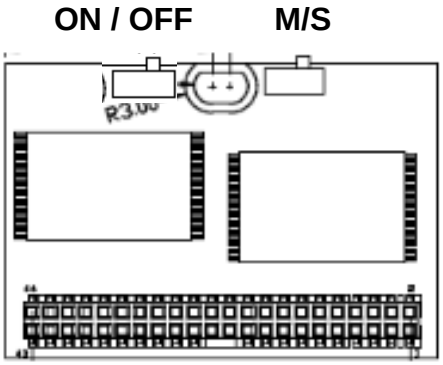

Figure 3: EDC 4000 Plus 44P Horizontal A type Write protect and Master/Slave switch

3.Pin Assignment

See Table 1 for EDC4000 Plus pin assignments.

Table 1: EDC4000 Plus Pin Assignments

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	40-pin VCC[1]	Supply Voltage
				44pin KEY[1]	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
23	HIOW[3]	Host I/O Write	24	GND	Ground
	STOP[4]	Stop Ultra DMA burst			
25	HIOR[3]	Host I/O Read	26	GND	Ground
	HDMARDY[4]	Ultra DMA ready			
	HSTROBE[4]	Ultra DMA data strobe			
27	IORDY[3]	I/O Ready	28	CSEL	Master/Slave Select (Switch used)
	DDMARDY[4]	Ultra DMA ready			
	DSTROBE[4]	Ultra DMA data strobe			
29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
Pin No.	Name	Function	Pin No.	Name	Function
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2

37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41[2]	VCC	Supply Voltage	42[2]	VCC	Supply Voltage
43[2]	GND	Ground	44[2]	NC	Not Connected

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.

2. The 40-pin version does not contain pins 41-44.

NC = These pins are not connected internally.

3. Signal usage in PIO & Multiword DMA mode.

4. Signal usage in Ultra DMA mode.

4. Pin Description

Table 2 describes the pin descriptions for EDC4000 Plus

Table 2: EDC4000 Plus Pin Description

Pin Name	Pin No.	Description	I/O
Host side pins			
HRESET-	1	Host reset signal, High: Reset.	I
CS0-	37	Chip select CS0	I
CS1-	38	Chip select CS1	I
INTRQ	31	Host interrupt signal.	O
HIOR-[3]	25	I/O read strobe signal.	I
HDMARDY-[4]		DMA ready during Ultra DMA data in burst	
HSTROBE[4]		Data strobe during Ultra DMA data out burst	
HIOW-[3]	23	I/O write strobe signal.	I
STOP[4]		Stop during Ultra DMA data bursts	
IOCS16-	32	Asserted in 16-bit access.	O
IORDY[3]	27	I/O Ready Signal	O
DDMARDY-[4]		DMA ready during Ultra DMA data out burst	

DSTROBE[4]		Data strobe during Ultra DMA data in burst	
HDB[15:0]	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	Host data bus	I/O
HAB[2:0]	33, 35, 36	Host Address bus	I/O
CSEL-	28	Master/Slave select signal (cable select signal). Low: Device operates as a master, High: Device operates as a slave. Switch used.	I
DASP-	39	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.	I/O
PDIAG-	34	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.	I/O
DMARQ	21	DMA Request.	O
DMACK-	29	DMA Acknowledge.	I
Power and Ground			
VCC	20[1], 41[2], 42[2]	Connect to VCC	VCC
GND	2, 19, 22, 24, 26, 30, 40, 43[2]	Connect to GND.	GND
Other pins			
NC	44[2]	Not used. Please do not connect.	N/A

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.

2. The 40-pin version does not contain pins 41-44.

   NC = These pins are not connected internally.

3. Signal usage in PIO & Multiword DMA mode.

4. Signal usage in Ultra DMA mode.

5. Specifications

5.1 CE and FCC Compatibility

EDC4000 Plus conforms to CE and FCC requirements.

5.2 RoHS Compliance

EDC4000 Plus is fully compliant with RoHS directive.

5.3 Environmental Specifications

5.3.1 Temperature Ranges

Operating Temperature Range: 0°C to +70°C (Stanard)

-40°C to +85°C (Industrial)

Storage Temperature Range: -55°C to +95°C

5.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.3.3 Shock and Vibration

Table 3: Shock/Vibration Test for EDC4000 Plus

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2 KHz, 20 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 g, 3 axes	IEC 68-2-27

5.3.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various EDC4000 Plus configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 4: EDC4000 Plus MTBF

Product	Condition	MTBF (Hours)
EDC4000 Plus	Telcordia SR-332 GB, 25°C	3,000,000

5.4 Mechanical Dimensions

40pin Vertical (DE0H-XXXD5XXX)

Mechanical Dimension: 60.2/6.4/27.8 mm±0.1(W/T/H)

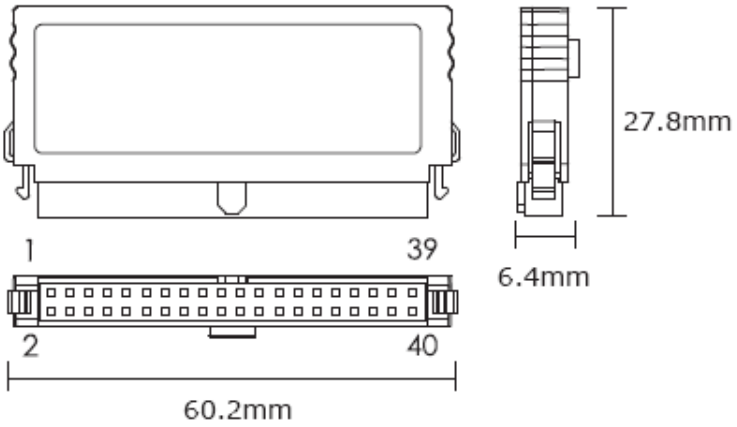

Figure 4 Mechanical Dimension of EDC 4000 Plus 40pin

44pin Vertical (DE4H-XXXD5XXX)

Mechanical Dimension: 50.3/5.8/27.3 mm ± 0.1mm(W/T/H)

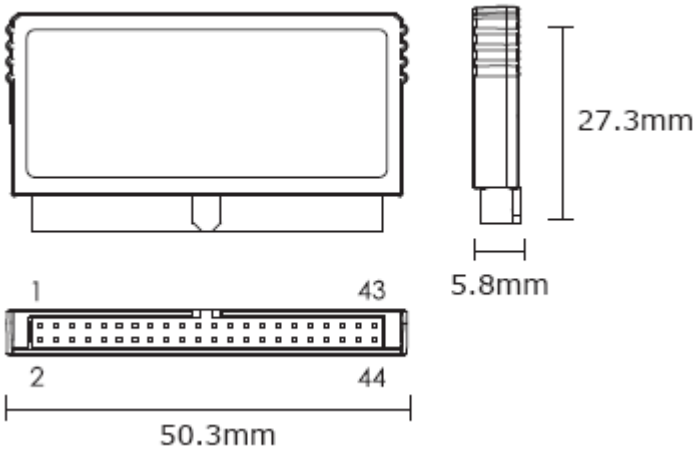

Figure 5 Mechanical Dimension of EDC 4000 Plus 44pin

44pin Horizontal (DE4PA-XXXD5XXX)

A

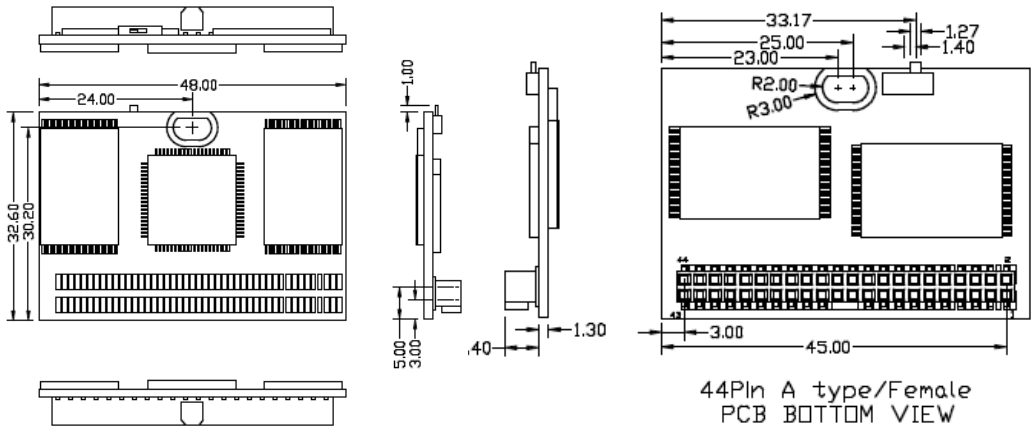

Figure 6: Mechanical Dimension of EDC 4000 Plus 44-pin (Horizontal Female Type A)

44pin Horizontal (DE4PB-XXX5XXXX)

B

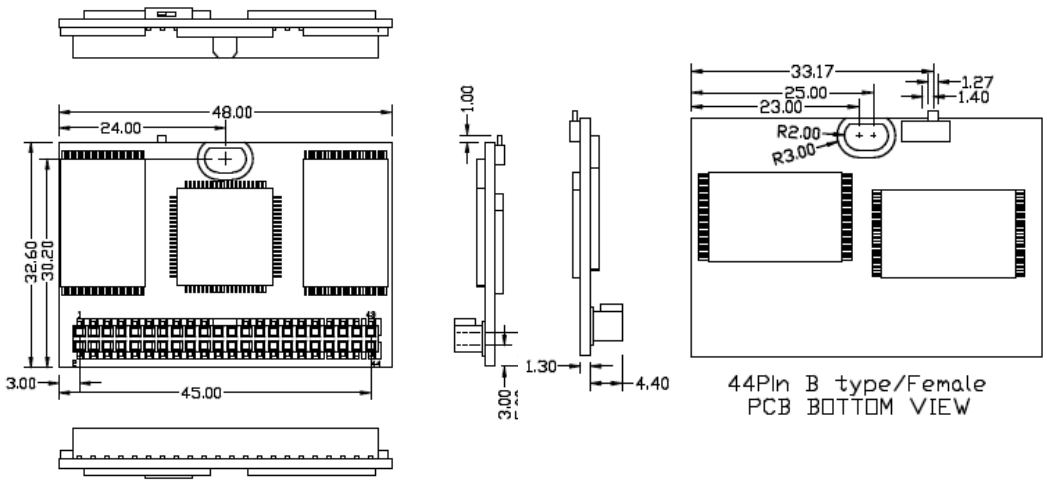

Figure 7: Mechanical Dimension of EDC 4000 Plus 44-pin (Horizontal Female Type B)

44pin Horizontal (DE4PC-XXXD5XXX)

C

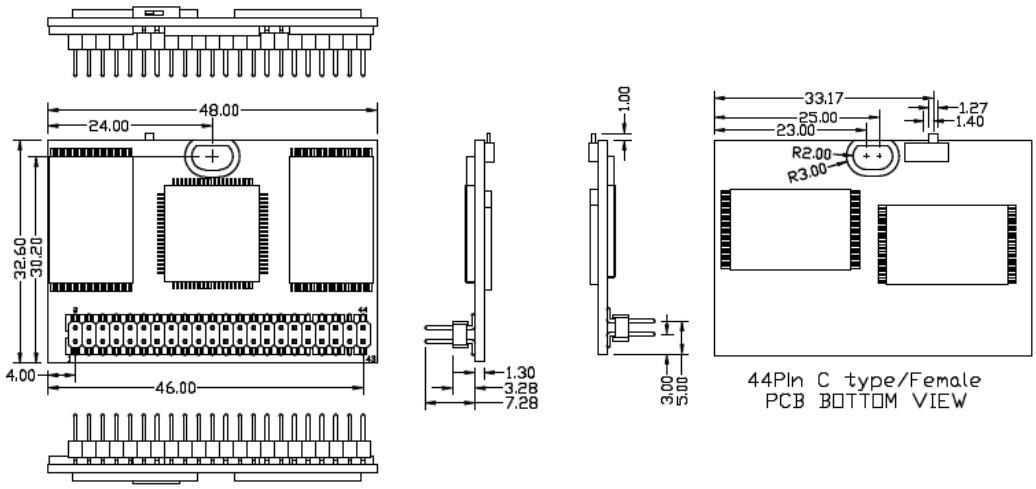

Figure 8: Mechanical Dimension of EDC 4000 Plus 44-pin (Horizontal Male Type C)

44pin Horizontal (DE4PD-XXXD5XXX)

D

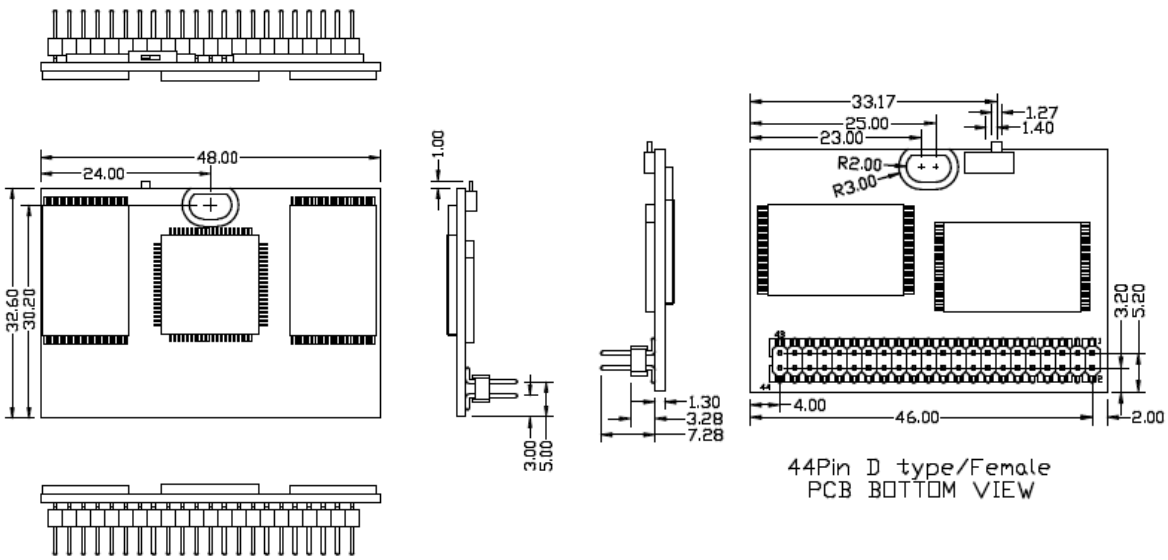

Figure 9: Mechanical Dimension of EDC 4000 Plus 44-pin (Horizontal Male Type D)

44pin Horizontal (DE4PE-XXXD5XXX)

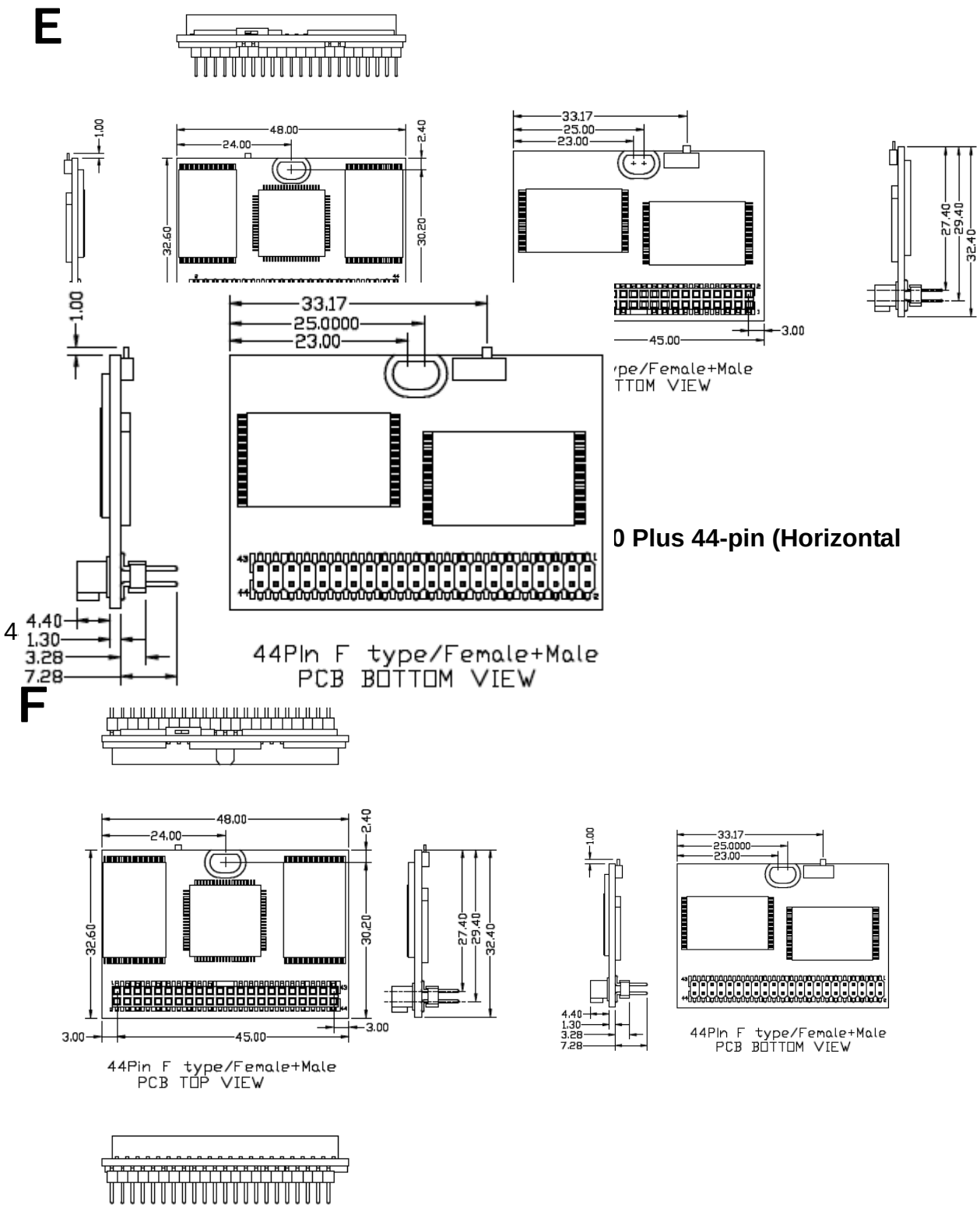

Figure 11: Mechanical Dimension of EDC 4000 Plus 44-pin (Horizontal Male/Female Type F)

5.5 Electrical Specifications

DC Characteristic

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+5 DC ± 5%	V
		+3.3 DC ± 0.3	

Timing Specifications

Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in Table 5.

Table 5: Attribute Memory Read Timing

Speed Version		300ns	
Item	**Symbol**	**Min (ns)**	**Max (ns)**
Read cycle time	tc(R)	300	
Address access time	ta(HA)		300
Card enable access time	ta(CEx)		300
Output enable access time	ta(HOE)		150
Output disable time from CE	tdis(CEx)		100
Output disable time from OE	tdis(HOE)		100
Address setup time	tsu(HA)	30	
Output enable time from CE	ten(CEx)	5	
Output enable time from OE	ten(HOE)	5	
Data valid from address change	tv(HA)	0	

Note: All times intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Card to the system. The CEx# signal or both the HOE# signal and the HWE# signal are deasserted between consecutive cycle operations.

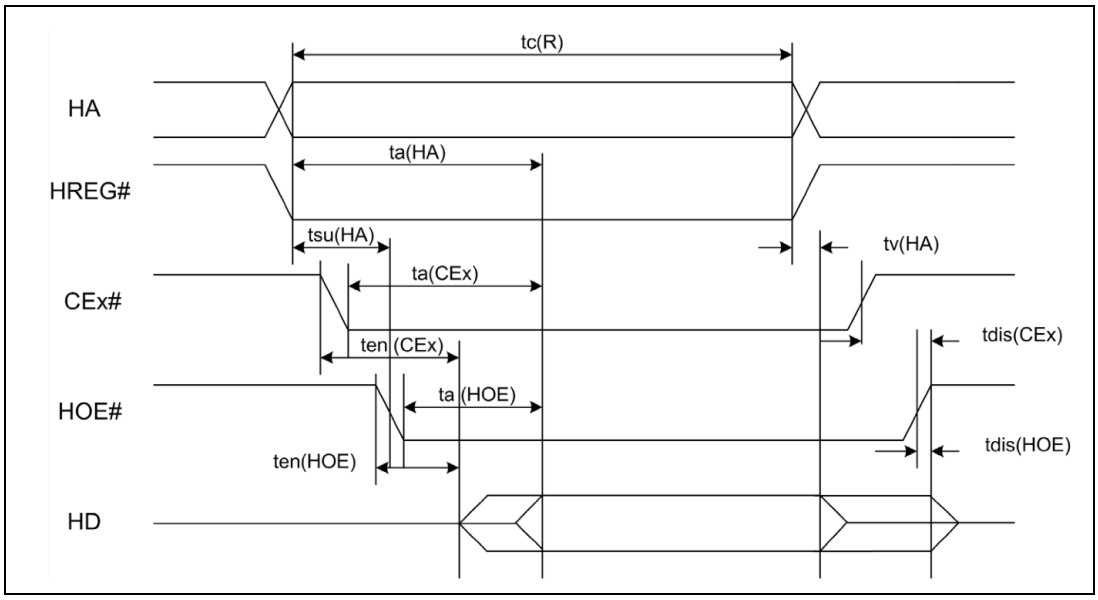

Figure 12: Attribute Memory Read Timing Diagram

Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250ns. Defined timing specifications are shown in Table 6.

Table 6: Configuration Register (Attribute Memory) Write Timing

Speed Version		**250ns**	
Item	**Symbol**	**Min (ns)**	**Max (ns)**
Write cycle time	tc(W)	250	
Write pulse width	tw(HWE)	150	
Address setup time	tsu(HA)	30	
Write recovery time	trec(HWE)	30	
Data setup time for WE	tsu(HD-WEH)	80	
Data hold time	th(HD)	30	

Note: All times intervals are recorded in nanoseconds. HD refers to data provided by the system to the CompactFlash Card.

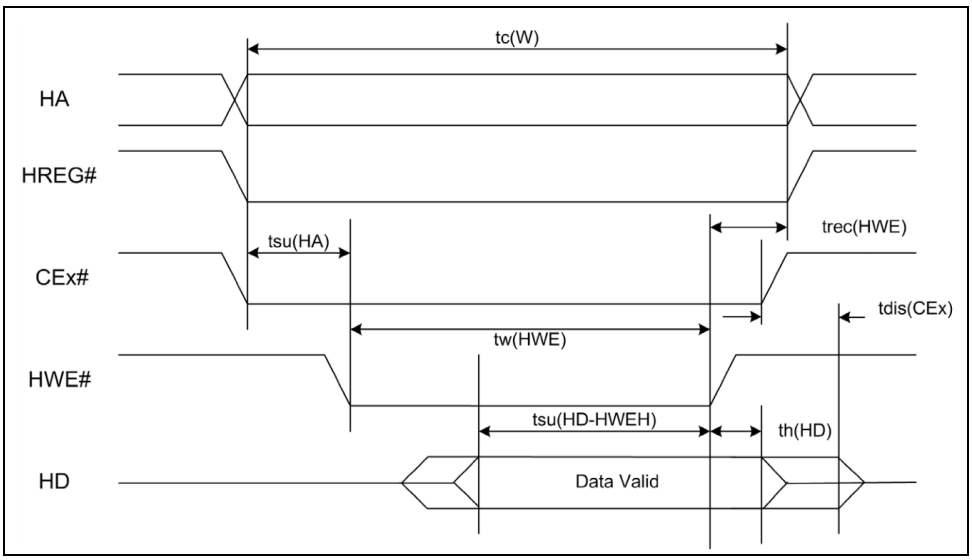

Figure 13 Configuration Register (Attribute Memory) Write Timing Diagram

Common Memory Read Timing Specification

Table 7: Common Memory Read Timing

Cycle Time Mode:		250ns		120ns		100ns		80ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output enable access time	ta(HOE)		125		60		50		40
Output disable time from HOE#	tdis(HOE)		100		60		50		40
Address setup time	tsu(HA)	30		15		10		10	
Address hold time	th(HA)	20		15		15		10	
CEx# setup before HOE#	tsu(CEx)	5		5		5		5	
CEx# hold following HOE#	th(CEx)	20		15		15		10	
Wait delay falling from HOE#	tv(IORDY-HOE)		35		35		35		Na[1]
Data setup for wait release	tv(IORDY)		0		0		0		Na[1]
Wait width time[2]	tw(IORDY)		350		350		350		Na[1]

Note: 1) IORDY is not supported in this mode.

2) The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All times intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Card to the system. The IORDY signal can be ignored when the HOE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait

Width time can be determined from the Card Information Structure (CIS). Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification.

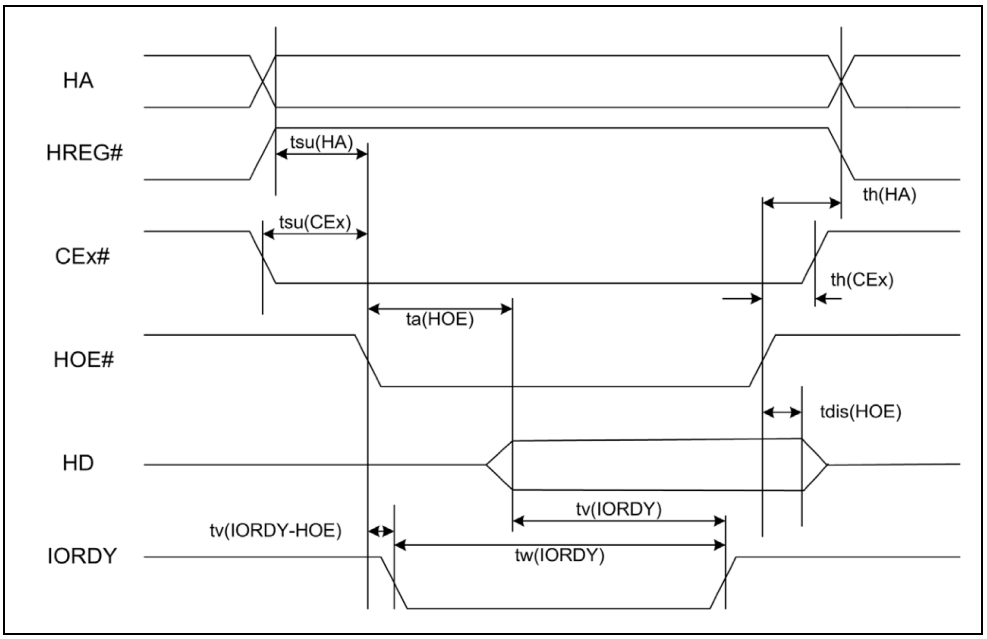

Figure 14 Common Memory Read Timing Diagram

Common Memory Write Timing Specification

Table 8: Common Memory Write Timing

Cycle Time Mode:		**250ns**		**120ns**		**100ns**		**80ns**	
Item	**Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before HWE#	tsu(HD-WEH)	80		50		40		30	
Data Hold following HWE#	th(HD)	30		15		10		10	
HWE# Pulse Width	tw(HWE)	150		70		60		55	
Address Setup Time	tsu(HA)	30		15		10		10	
CEx# Setup before HWE#	tsu(CEx)	5		5		5		5	
Write Recovery Time	trec(HWE)	30		15		15		15	
Address Hold Time	th(HA)	20		15		15		15	
CE Hold following HWE#	th(CEx)	20		15		15		10	
Wait Delay Falling from HWE#	tv(IORDY-WE)		35		35		35		Na[1]
HWE# High from Wait Release	tv(IORDY)	0		0		0		Na[1]	
Wait width time[2]	tw(IORDY)		350		350		350		Na[1]

Note: 1) IORDY is not supported in this mode.

2) The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec Cycle Time) total load. All times intervals are recorded in nanoseconds. HD refers to data provided by the CompactFlash Card to the system. The IORDY signal can be ignored when the HWE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS). Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification.

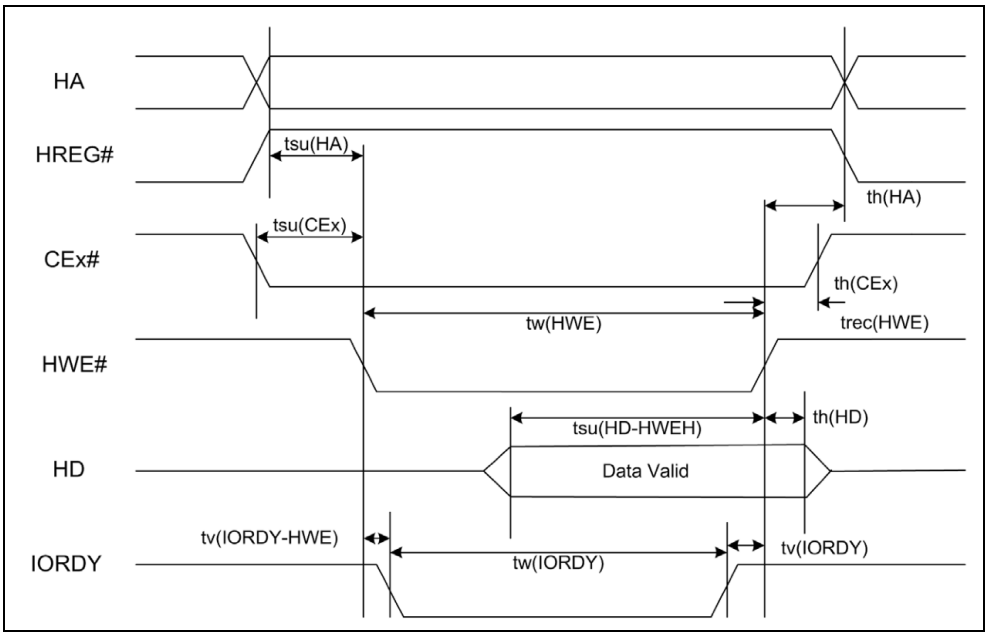

Figure 15 Common Memory Write Timing Diagram

I/O Input (Read) Timing Specification

Table 9: I/O Read Timing

Cycle Time Mode:		**250 ns**		**120 ns**		**100 ns**		**80 ns**	
Item	**Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after HIOE#	td(HIOE)		100		50		50		45
Data Hold following HIOE#	th(HIOE)	0		5		5		5	
HIOE# Width Time	tw(HIOE)	165		70		65		55	
Address Setup before HIOE#	tsuA(HIOE)	70		25		25		15	
Address Hold following HIOE#	thA(HIOE)	20		10		10		10	

CEx# Setup before HIOE#	tsuCEx (HIOE)	5		5		5		5	
CEx# Hold following HIOE#	thCEx (HIOE)	20		10		10		10	
HREG# Setup before HIOE#	tsuHREG (HIOE)	5		5		5		5	
HREG# Hold following HIOE#	thHREG (HIOE)	0		0		0		0	
Wait Delay Falling from HIOE#[2]	tdIORDY (HIOE)		35		35		35		Na[1]
Data Delay from Wait Rising[2]	td(IORDY)		0		0		0		Na[1]
Wait Width Time[2]	tw(IORDY)		350		350		350		Na[1]

Note: 1) IORDY is not supported in this mode.

2) Maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the CompactFlash Card to the system. Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification.

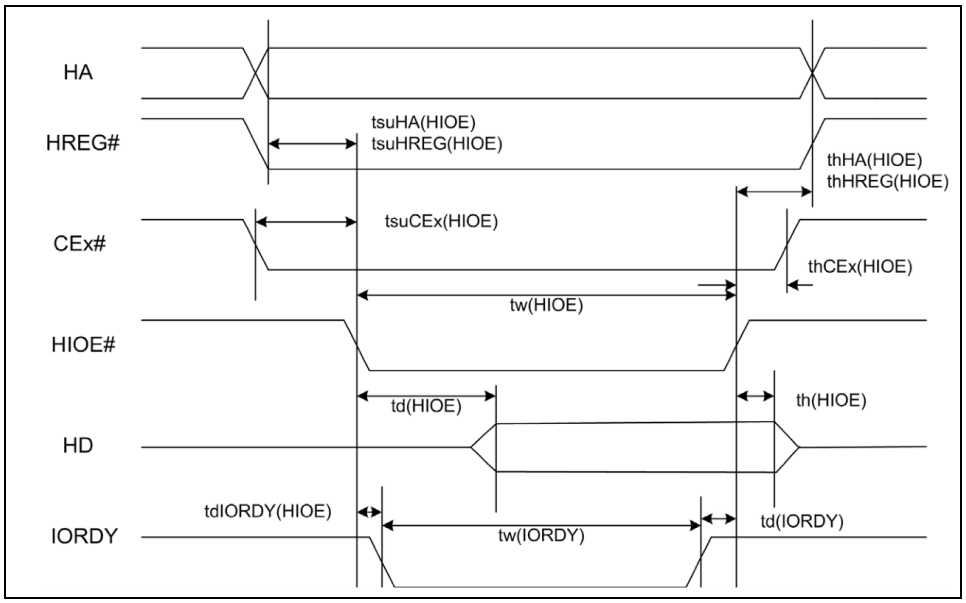

Figure 16 I/O Read Timing Diagram

Timing Specification

Table 10: I/O Write Timing

Cycle Time Mode:		250ns		120ns		100ns		80ns	
Item	**Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before HIOW#	tsu(HIOW)	60		20		20		15	
Data Hold following HIOW#	th(HIOW)	30		10		5		5	
HIOW# Width Time	tw(HIOW)	165		70		65		55	
Address Setup before HIOW#	tsuHA(HIOW)	70		25		25		25	
Address Hold following HIOW#	thHA(HIOW)	20		20		10		10	
CEx# Setup before HIOW#	tsuCEx(HIOW)	5		5		5		5	
CEx# Hold following HIOW#	thCEx(HIOW)	20		20		10		10	
HREG# Setup before HIOW#	tsuHREG(HIOW)	5		5		5		5	
HREG# Hold following HIOW#	thHREG(HIOW)	0		0		0		0	
Wait Delay Falling from HIOW#[2]	tdIORDY(HIOW)		35		35		35		Na[1]
HIOW# high from Wait high[2]	tdrHIOW(IORDY)	0		0		0		Na[1]	
Wait Width Time[2]	tw(IORDY)		350		350		350		Na[1]

Note: 1) IORDY is not supported in this mode.

2) The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOW# high is 0 nsec, the minimum HIOW# width is still met. HD refers to data provided by the CompactFlash Card to the system. Although adhering to the PCMCIA specification of 12 µs, the Wait Width time is intentionally lower in this specification.

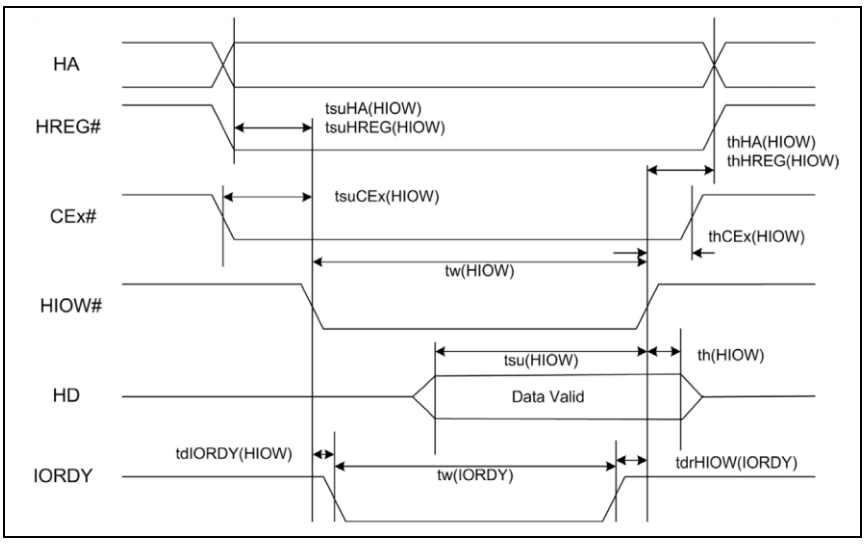

Figure 17 I/O Write Timing Diagram

True IDE PIO Mode Read/Write Timing Specification

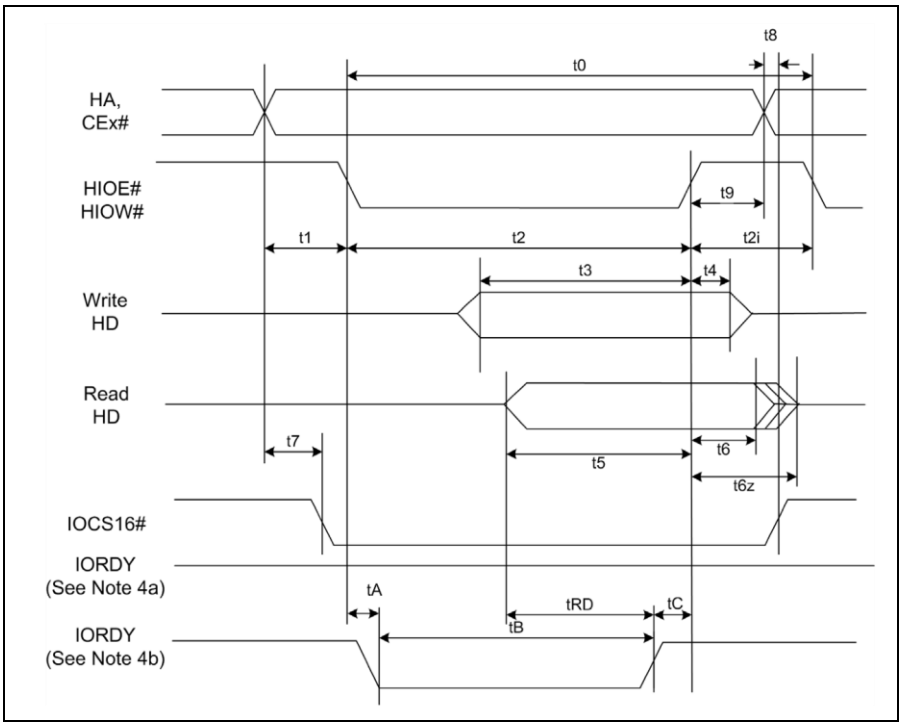

Figure 18 Read/Write Timing Diagram, PIO Mode

Note: 1) Device address comprises CE1#, CE2#, and HA[2:0].

2) Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit).

3) IOCS16# is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.

4) The negation of IORDY by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after tA from the assertion of HIOE# or HIOW#. The assertion and negation of IORDY is described in the following three cases.

(a) The device never negates IORDY: No wait is generated.

(b) Device drives IORDY low before tA: a wait is generated. The cycle is completed after IORDY is reasserted. For cycles in which a wait is generated and HIOE# is asserted, the device places read data on D15-D00 for tRD before IORDY is asserted.

Table 11: Read/Write Timing Specifications, PIO Mode 0-4

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t0	Cycle time (min.)[1]	600	383	240	180	120
t1	Address valid to HIOE# /	70	50	30	30	25

	HIOW# setup (min.)					
t2	HIOE# / HIOW# (min.)[1]	165	125	100	80	70
t2	HIOE# / HIOW# (min.) Register (8-bit)[1]	290	290	290	80	70
t2i	HIOE# / HIOW# recovery time (min.)	-	-	-	70	25
t3	HIOW# data setup (min.)	60	45	30	30	20
t4	HIOW# data hold (min.)	30	20	15	10	10
t5	HIOE# data setup (min.)	50	35	20	20	20
t6	HIOE# data hold (min.)	5	5	5	5	5
t6Z	HIOE# data tristate (max.)[2]	30	30	30	30	30
t7	Address valid to IOCS16# assertion (max.)[4]	90	50	40	n/a	n/a
t8	Address valid to IOCS16# released (max.)[4]	60	45	30	n/a	n/a
t9	HIOE# / HIOW# to address valid hold	20	15	10	10	10
tRD	Read data valid to IORDY active (min.), if IORDY initially low after tA	0	0	0	0	0
tA	IORDY setup time[3]	35	35	35	35	35
tB	IORDY pulse width (max.)	1250	1250	1250	1250	1250
tC	IORDY assertion to release (max.)	5	5	5	5	5

Note: All timings are in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met.

1) Where t0 denotes the minimum total cycle time; t2 represents the minimum command active time; t2i is the minimum command recovery time or command inactive time. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements for t0, t2, and t2i are met. The minimum total cycle time requirement is greater than the sum of t2 and t2i, implying that a host implementation can extend either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identity data. A CompactFlash Card implementation supports any legal host implementation.

2) This parameter specifies the time from the negation edge of the HIOE# to

the time that the CompactFlash Card (tri-state) no longer drives the data bus.

3) The delay originates from HIOE# or HIOW# activation until the state of IORDY is first sampled. If IORDY is inactive, the host waits until IORDY is active before the PIO cycle is completed. When the CompactFlash Storage Card is not driving IORDY, which is negated at tA after HIOE# or HIOW# activation, then t5 is met and tRD is inapplicable. When the CompactFlash Card is driving IORDY, which is negated at the time tA after HIOE# or HIOW# activation, then tRD is met and t5 is inapplicable.

4) Both t7 and t8 apply to modes 0, 1, and 2 only. For other modes, this signal is invalid.

5) IORDY is not supported in this mode.

True IDE Multiword DMA Mode Read/Write Timing Specification

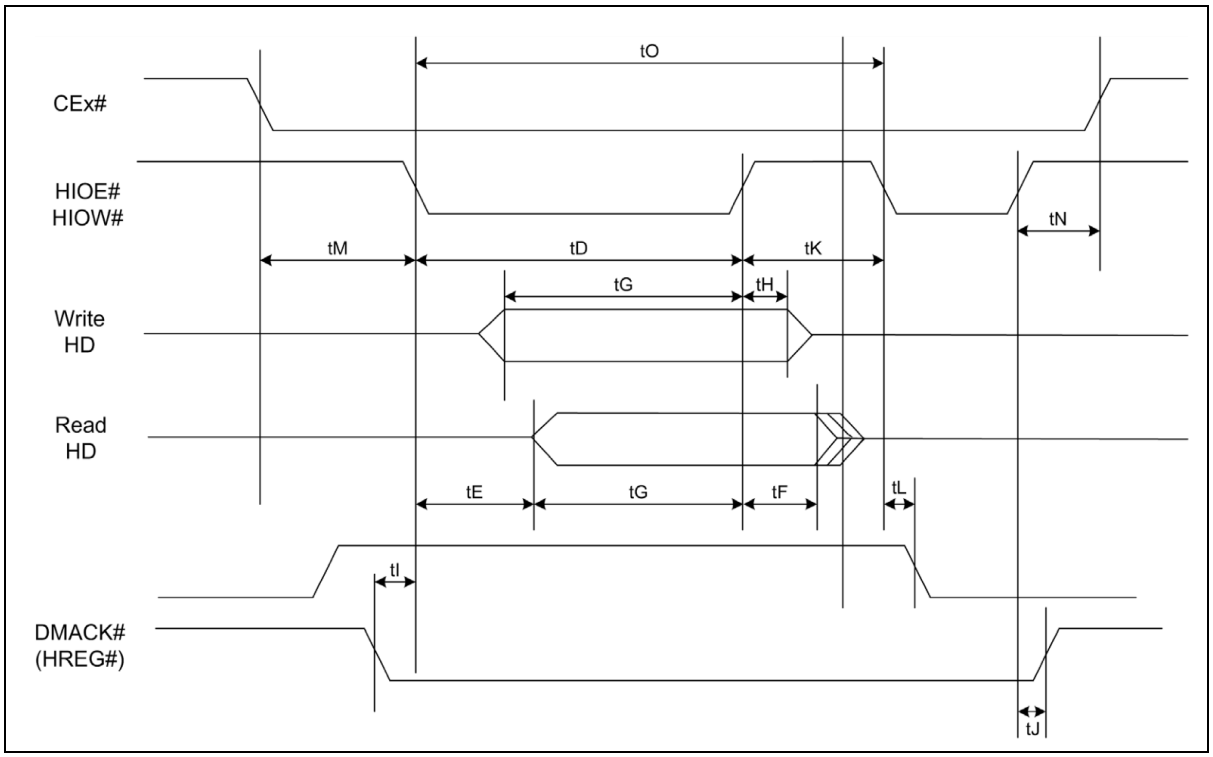

Figure 19 Read/Write Timing Diagram, Multiword DMA Mode

Note: 1) If a card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ during the time from the start of a DMA transfer cycle (to suspend DMA transfers in progress) and reassertion of the signal at a relatively later time to continue DMA transfer operations.

2. The host may negate this signal to suspend the DMA transfer in progress.

Table 12: Read/Write Timing Specifications, Multiword DMA Mode 0-2

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t0	Cycle time (min.)	480	150	120
tD	HIOE# / HIOW# assertion width (min.)	215	80	70
tE	HIOE# data access (max.)	150	60	50
tF	HIOE# data hold (min.)	5	5	5
tG	HIOE# / HIOW# data setup (min.)	100	30	20
tH	HIOW# data hold (min.)	20	15	10
tI	HREG# to HIOE# / HIOW# setup (min.)	0	0	0
tJ	HIOE# / HIOW# to HREG# hold (min.)	20	5	5
tKR	HIOE# negated width (min.)	50	50	25
tKW	HIOW# negated width (min.)	215	50	25
tLR	HIOE# to DMARQ delay (max.)	120	40	35
tLW	HIOW# to DMARQ delay (max.)	40	40	35
tM	CEx# valid to HIOE# / HIOW#	50	30	25
tN	CEx# hold	15	10	10

Note: Where t0 is the minimum total cycle time and tD is minimum command active time, whereas tKR and tKW are minimum command recovery time or command inactive time for input and output cycles, respectively. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements of t0, i.e. tD, tKR, and tKW, must be met. The minimum total cycle time requirement exceeds the sum of tD and tKR or tKW for input and output cycles, respectively, implying that a host implementation can extend either or both tD and tKR or tKW as deemed necessary to ensure that t0 equals or exceeds the value reported in the device's identity data. A CompactFlash Card implementation supports any legal host implementation.

True IDE Ultra DMA Mode Read/Write Timing Specification

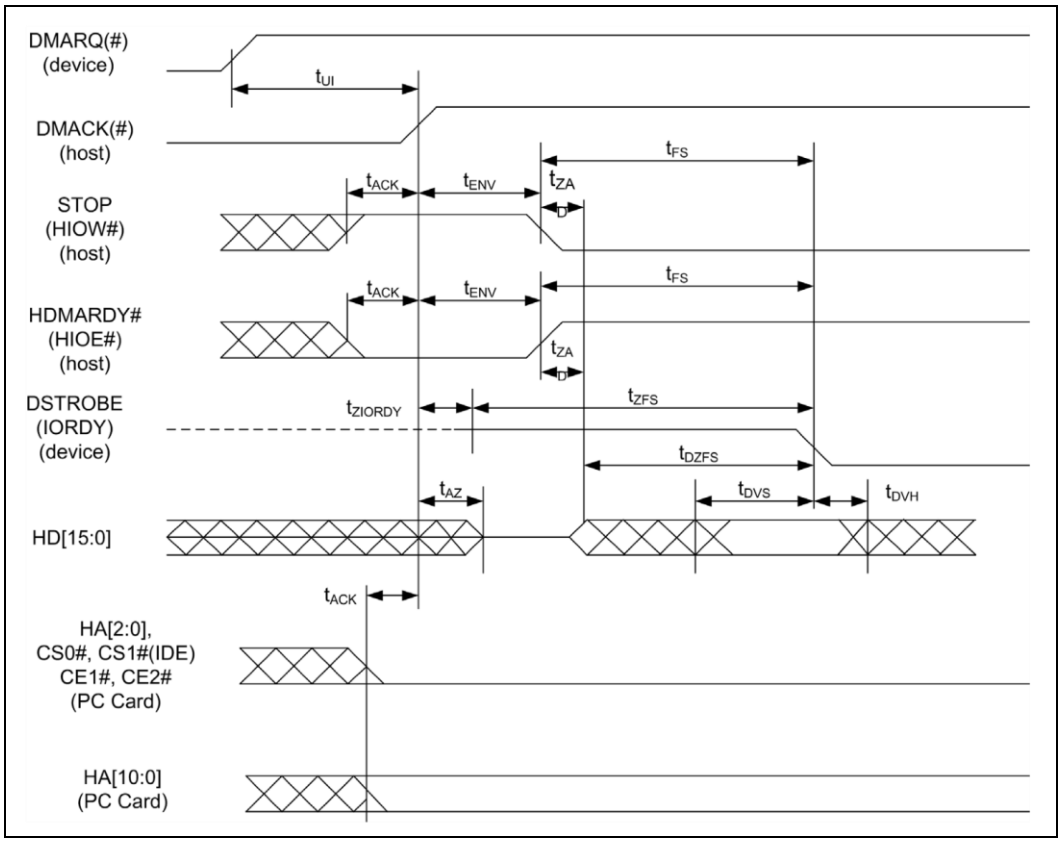

Figure 20 Ultra DMA Mode Data-in Burst Initiation Timing Diagram

Note: 1) All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.

2) The definitions for the IORDY:DDMARDY#:DSTROBE, HIOE#: HDMARDY#: HSTROBE and HIOW#: STOP signal lines are not in effect until DMARQ(#) and DMACK(#) are asserted. Notably, HA[2:0], CS0# and CS1# are True IDE mode signal definitions, and HA[10:0], CE1# and CE2# are PC Card mode signals. The Bus polarity of DMACK(#) and DMARQ(#) is based on the active interface mode.

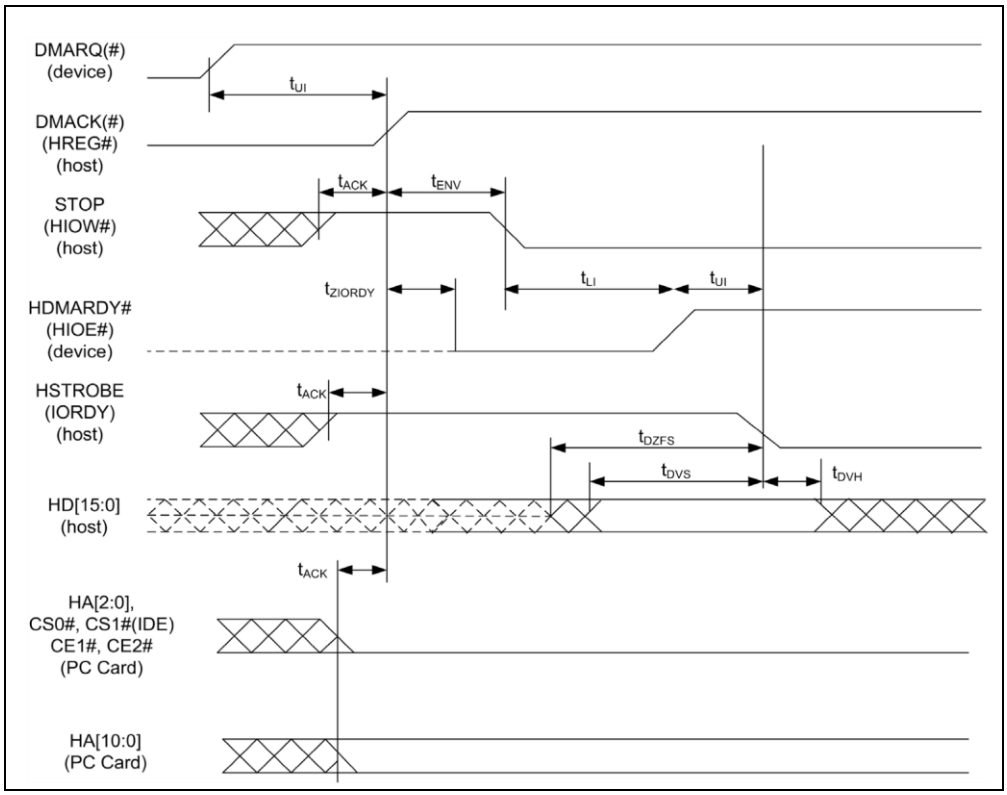

Figure 21 Ultra DMA Mode Data-out Burst Initiation Timing Diagram

Note: 1) All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.

2) Definitions for STOP, DDMARDY#, and HSTROBE signal lines are not in effect until DMARQ(#) and DMACK(#) are asserted. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

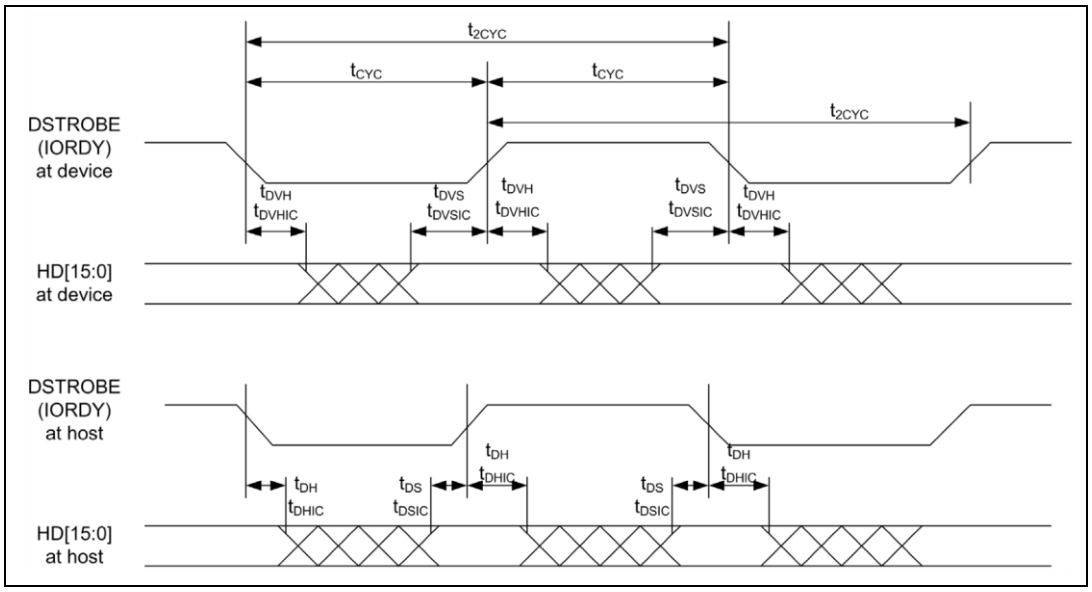

Figure 22 Sustained Ultra DMA Mode Data-in Burst Timing Diagram

Note: HD[15:0] and IORDY signals are shown at both the host and device to emphasize that neither cable settling time nor cable propagation delay allow data signals to be considered stable at the host until after they are driven by the device.

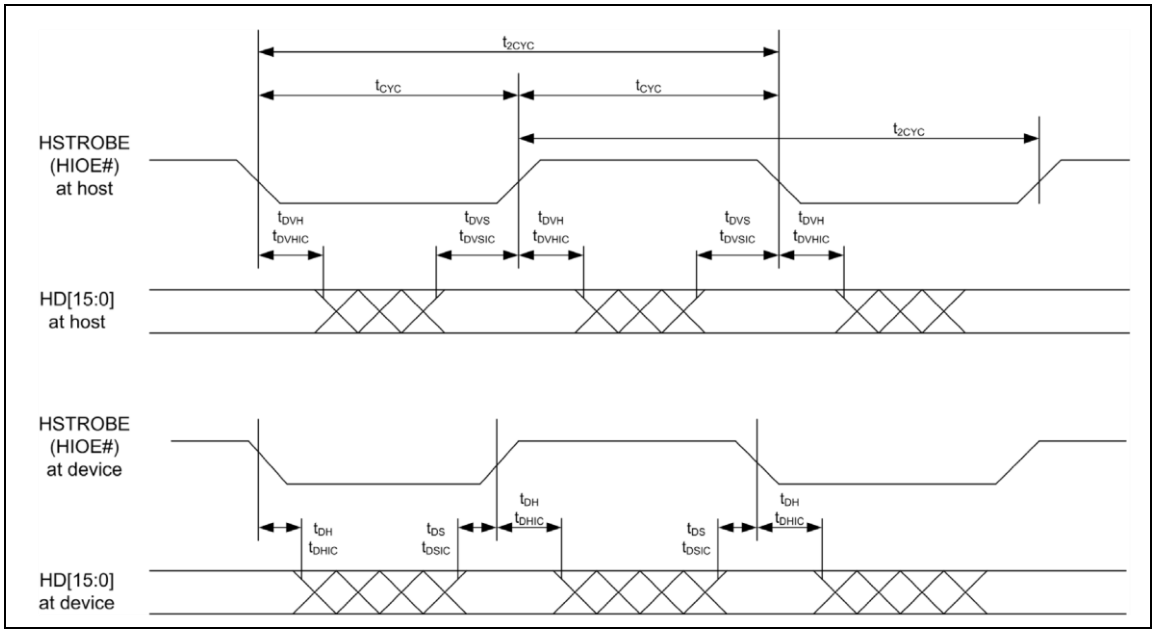

Figure 23 Sustained Ultra DMA Mode Data-out Burst Timing Diagram

Note: Data (HD[15:0]) and HSTROBE signals are shown at both the device and host to emphasize that neither cable settling time nor cable propagation delay allow for data signals to be considered stable at the device until after they are driven by a host.

Table 13: Timing Diagram, Ultra DMA Mode 0-4

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
$t_{2CYCTYP}$	Typical sustained average two cycle time	240	-	160	-	120	-	90	-	60	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	115	-	86	-	57	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	170	-	130	-	120
t_{LI}	Limited interlock time	0	150	0	150	0	150	0	100	0	100
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60

t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	50	-	50	-

5.6 Transfer Function

5.6.1 I/O Transfer function

The I/O transfer to or from the EDC4000 Plus can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal –IOIS16 is asserted by the EDC4000 Plus. Otherwise, the –IOIS16 signal is de-asserted. When a 16 bit transfer is attempted and the –IOIS16 signal is not asserted by the EDC4000 Plus, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The EDC4000 Plus permits both 8 and 16 bit accesses to all of its I/O addresses, so –IOIS 16 is asserted for add address to which the EDC4000 Plus responds. The EDC4000 Plus may request the host to extend the length of an input cycle until data ready by asserting the –WAIT signal at the start of the cycle.

Table 14*: PCMCIA Mode I/O Function*

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15~D8	D7~D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte

I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

5.6.2 Common Memory Transfer Function

The Common Memory transfer to or from EDC4000 Plus can be either 8 or 16 bits. The EDC4000 Plus permits both 8 and 16 bit access to all of its Common Memory addresses. The EDC4000 Plus request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the –WAIT signal at the start of the cycle.

Table 15: Common Memory Function

Function Code	**-REG**	**-CE2**	**-CE1**	**A0**	**-OE**	**-WE**	**D15~D8**	**D7~D0**
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Output Access (16bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

5.6.3 True IDE Mode I/O Transfer Function

The EDC4000 Plus can be configured in a True IDE Mode of operation. The EDC4000 Plus is configured in this mode only when –OE input signal is grounded by the host during the power off to power on cycle.

Table 16: True IDE Mode I/O Function

Function Code	-CS1	-CS0	-A0~A2	-DMACK	-IORD	-IOWR	D15~D8	D7~D0
Invalid Mode	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data In
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte In	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 1		Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 2		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address	L	H	7h	H	L	H	High Z	Data Out

Note1: In Ultra DMA Data Register Write mode the signals –IORD, -IOWR and IORDY are redefined

and used as follows: -IORD as HSTROBE, -IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE.

Note2: In Ultra DMA Data Register Read mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as –HDMARDY H, -IOWR as STOP and IORDY as DSTROBE. Data transfer with each edge of DSTROBE.

5.7 Configuration Register

5.7.1 Configuration Option Register (200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the EDC4000 Plus.

Table 17: Configuration Option Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevelREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 18: Information for Configuration Option Register

Name	Description
SRSET	Soft Reset: Setting this bit to one (1), waiting the minimum reset time and returning to zero(0) places the EDC4000 Plus in the reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the EDC4000 Plus in the same un-configured, Reset state as following power-up and hardware reset. This bit is PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.
LevelREQ	This bit is set to one (1) then Level Mode Interrupt is selected, and zero (0) then Pulse Mode is selected. Set to zero (0) by Reset.
Conf5-0	Configuration Index: Set to zero (0) by reset. It is used to select operation mode of the EDC4000 Plus as shown below

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and shall be written as zero(0).

Table 19:EDC4000 Plus Configuration

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary

0	0	0	0	1	0	Primary I/O Mapped, 1F0h~1F7h/3F6h ~ 3F7h
0	0	0	0	1	1	Secondary I/O Mapped, 170h~177h/376h ~ 377h

5.7.2 Card Configuration and Status Register (202h in Attribute Memory)

The Card configuration and Status Register contains information about the Card's condition.

Table 20: Card Configuration and Status Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PweDwn	0	0

Table 21: Information for Card Configuration and Status Register

Name	Description
Changed	Indicates that one or both of the Pin Replacement register CReady. Or CWProt bits are set to one(1). When the changed bit is set. –STSCHG Pin 46 us held low if the SigChg bit is a One(1) and the EDC4000 Plus is configured for I/O interface.
SigChg	This bit is set and reset by the host to enable and disable a state-change "single" from the Status Register, the Changed bit controls pin 46, the Changed Status single. If no state change single is descried, this bit is set to zero(0) and pin46 (-STSCHG) single is then held high while the EDC4000 Plus is configured for I/O.
IOis8	The host sets this bit to one (1) if the EDC4000 Plus is to be configured in an 8 bit I/O Mode. The EDC4000 Plus is always configured for both 8 and 16 bit I/O, so this bit is ignored.
PwrDwn	This bit indicates whether the host requests EDC4000 Plus to be in the power saving or active mode. When the bit is one (1), the EDC4000 Plus enter a power down mode. The PwrDwn is zero (0), the host is requesting the EDC4000 Plus to enter the active mode. The PCMCIA READY value becomes false (busy) when this bit is changed. READY shall not become true (ready) until the power state requested has been entered. The EDC4000 Plus automatically powers down when it is idle and powers back up when it receives a command.

Int	This bit represents the internal state of the interrupt request. This value is available whether or not the I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is a zero (0).

5.7.3 Pin Replacement register (204h in Attribute Memory)

Table 22: Pin Replacement Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CReady	0	1	1	RReady	0
Write	0	0	CReady	0	0	0	MReady	0

Table 23: Information for Pin Replacement Register

Name	Description
CReady	This bit is set to one (1) when the bit RReady changes state. This bit can also be written by the host.
RReady	This bit is used to determine the internal state of the READY signal. This bit may be used to determine the state of the READY signal as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask(MReady) for writing the corresponding bit CReady.
MReady	This bit acts as a mask for writing corresponding bit CReady.

5.7.4 Socket and Copy Register (206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is used for identification of the card from the other card.

Table 24: Socket and Copy Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	Obsolete (Drive #)	0	0	0	0
Write	0	0	0	Obsolete (Drive #)	X	X	X	X

Table 25: Information for Socket and Copy Register

Name	Description
Obsolete(Drive #)	This bit is obsolete and should be written as 0.

5.8 Software Interface

5.8.1 CF-ATA Drive Register Set Definition and Protocol

The EDC4000 Plus can be configured as a high performance I/O device through:

a) The standard PC-AT disk I/O address 1F0h-1F7h, 3F6h-3F7h (primary) or 170h-177h, 376h-377h (secondary) with IRQ14 (or other available IRQ).
b) Any system decode 16 byte I/O block using any available IRQ.
c) Memory space

The communication to or from the card is done using the Task File register, which provide all the necessary register for control and status information related to the storage medium. The PCMCIA interface connects peripherals to the host using four register mapping methods.

Table 26: I/O Configuration

Standard Configurations			
Config Index	I/O or Memory	Address	Description
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	XX0h-XXFh	I/O Mapped 16 Contiguous Registers
2	I/O	1F0h-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170h-177h, 376h-377h	Secondary I/O Mapped

5.8.2 I/O Primary and Secondary Address Configurations

Table 27: Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)h	0	0	0	1	Error Register	Features	1,2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	

0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alt Status	Device Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Note 1) Register 0 is accessed with –CE1 low and –CE2 low (and A0=Don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with –CE1 low and –CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers, which lie at offset 1. When accessed twice as byte register with –CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

Note2) A byte access to register 0 with –CE1 high and –CE2 low access the error (read) or feature (write) register.

5.8.3 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the card, the registers are accessed in the block of I/O space decoded by the system as follows:

Table 28: Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Note
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Feature	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Note 1) Register 0 is accessed with –CE1 low and –CE2 low (and A0=Don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with –CE1 low and –CE2 high. Note that the address space of this

word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with –CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

Note 2) A byte access to register 0 with –CE1 high and –CE2 low access the error (read) or feature (write) register.

Note 3) Address lines that are not indicated are ignored by the card for accessing all the registers in this table.

5.8.4 Memory Mapped Addressing

When the card registers are accessed via memory references, the register appears in the common memory space window: 0-2K bytes as follows:

Table 29: Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Note
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1,2
1	0	X	0	0	0	1	1	Error	Features	1,2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Feature	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd Rd Data	Odd WR	3

									Data	

Note 1) Register 0 is accessed with –CE1 low and –CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with –CE1 low and –CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with –CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte accesses to register 0 with –CE1 high and –CE2 low access the error (read) or feature (write) register.

Note 2) Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the register is byte accessed in the order 9 then 8 the data shall be transferred odd byte then even byte. Repeated byte accessed to register 8 or 0 shall access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 shall access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to register 8 then 9 shall access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

Note 3) Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 K byte memory window to the data register is provide so that hosts can perform memory block moves to the data register when the register lies in memory space.
Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction, Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the card. A word access to address at offset 8 shall provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the bus.

5.8.5 True IDE Mode Addressing

When the EDC4000 Plus is configured in the True IDE mode, the I/O decoding is as follows:

Table 30: True IDE Mode I/O Decoding

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit
1	1	X	X	X	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	1	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

5.8.6 CF-ATA Register

The following section describes the hardware registers used by the host software to issue commands to the EDC4000 Plus.

Note:

In accordance with the PCMCIA specification: each of the registers below that is located at an odd offset address may be accessed in the PC Card Memory or PC Card I/O modes at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when –CE1 is high and –CE2 is low unless –IOIS16 is high (not asserted by the card) and an I/O cycle us being performed.

In True IDE Mode of operation, the size of the transfer is based solely on the register being addressed. All registers are 8 bit only except for the Data Register, which is normally 16 bits, but can be programmed to use 8 bit transfers for Non-DMA operations through the use of the Set Features command. The data register is also 8 bits during a portion of the Read Long and Write Long commands, which exist solely for historical reasons and should not be used.

Data Register

The Data Register is a 16 bit register, and it is used to transfer data blocks between the card and the host. This register overlaps the Error Register. This register can be accessed in word and byte mode.

Table 31: Data Register

Data Register															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

Table 32: Error Register

BBK	UNC	0	IDNF	0	ABRT	0	AMNF
D7	D6	D5	D4	D3	D2	D1	D0

Feature Register

This register provides information regarding features of the card that the host can utilize. This register is also accessed in PC Card modes on data D15-D8 during a write operation to Offset 0 with –CE2 low and –CE1 high.

Table 33: Feature Register

Feature Register							
D7	D6	D5	D4	D3	D2	D1	D0

Sector Count Register

This registers the number of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Table 34: Sector Count Register

Sector Count Register							
D7	D6	D5	D4	D3	D2	D1	D0

Sector Number Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for EDC4000 Plus data access for the subsequent command.

Table 35: Sector Number Register

Sector Number Register							
D7	D6	D5	D4	D3	D2	D1	D0

Cylinder Low Register

This Register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

Table 36: Cylinder Low Register

Cylinder Low Register							
D7	D6	D5	D4	D3	D2	D1	D0

Cylinder High Register

This Register contains the high order 8 bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

Table 37: Cylinder High Register

Cylinder High Register							
D7	D6	D5	D4	D3	D2	D1	D0

Device/Head Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing.

Table 38: Device/Head Register

1	LBA	1	DRV	HS3	HS2	HS1	HS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is set 1.

Bit6: LBA is a flag to select either Cylinder/Head/Sector or Logical Block Address mode. When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected.

Bit5: this bit is set 1.

Bit4: DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. Setting this bit to1 is obsolete in PCMCIA modes of operation.

Bit3: When operation in the Cylinder/Head/Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

Bit2: When operation in the Cylinder/Head/Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

Bit1: When operation in the Cylinder/Head/Sector mode, this is bit 1 of the head number. It is bit 25 in the Logical Block Address mode.

Bit0: When operation in the Cylinder/Head/Sector mode, this is bit 0 of the head

number. It is bit 24 in the Logical Block Address mode.

Status Register

These registers return the EDC4000 Plus status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not.

Table 39: Status Register

BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: the busy bit is set when the EDC4000 Plus has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit set to a 1.
Bit6: RDY indicates whether the device is capable of performing EDC4000 Plus operations. This bit is cleared at power up and remains cleared until the card is ready to accept a command.
Bit5: This bit, if set, indicates a write fault has occurred.
Bit4: This bit is set when the EDC4000 Plus is ready.
Bit3: The Data Request is set when the EDC4000 Plus requires that information be transferred either to or from the host through the Data register.
During the data transfer of DMA commands, the card shall not asserted DMARD unless either the BUST bit, the DRQ, or both are set to one.
Bit2: This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit1: This bit is always to 0.
Bit0: This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information description the error.

Device Control Register

This register is used to control the EDC4000 Plus interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY.

Table 40: Device Control Register

X	X	X	X	X	SW Rst	-IEn	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7-3: These bits are ignored.
Bit2: This bit is set to 1 in order to force the EDC4000 Plus to perform a Soft Reset

operation. This does not change PCMCIA Card Configuration Register as a hardware Reset does. The Card remains in Reset until this bit is reset to '0'.

Bit1: the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupt from the EDC4000 Plus are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit0: This bit is ignored.

Drive Address Register

This register is provide for compatibility with the AT disk drive interface.

Table 41: Drive Address Register

X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is unknown.

Bit6: this bit is – when a write operation is in progress; otherwise, it is 1.

Bit5: this bit is the negation of bit 3 in the Drive/Head register.

Bit4: this bit is the negation of bit 2 in the Drive/Head register.

Bit3: this bit is the negation of bit 1 in the Drive/Head register.

Bit2: this bit is the negation of bit 0 in the Drive/Head register.

Bit1: this bit is 0 when drive 1 is active and selected.

Bit0: this bit is 0 when the drive 0 is active and selected..

5.9 Hardware Reset(Only for Memory Card mode and I/O Card Mode)

Table 42: Timing Diagram, Hardware Reset

	Item	Min.	Max.	Normal	Unit
t_{SU}(RESET)	Reset Setup Time	20	-	-	ms
t_{REC}(VCC)	-CE Recover Time	1	-	-	us
t_{PR}	VCC rising up time	0.1	100	-	ms
t_{PF}	VCC falling down time	3	300	-	ms
t_{W}(RESET)	Reset pulse width	10	-	-	ms
t_{H}(Hi-ZRESET)		0	-	-	
t_{S}(Hi-ZRESET)		0	-	-	

Hardware Reset Timing

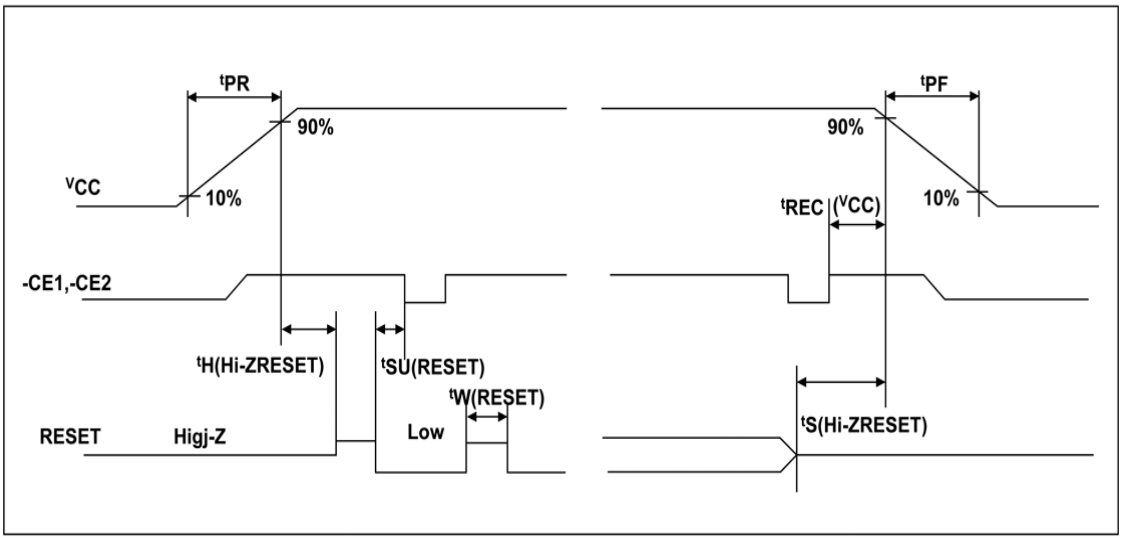

Figure 24 Timing Diagram, Hardware Reset

5.10 Power On Reset

When the VCC power reaches to 2.7V, the disk drive will be reset.

Table 43: Timing Diagram, Power On Reset

	Item	Min.	Max.	Normal	Unit	Note
t_{SU}(RESET)	-CE Setup Time	20	-	-	ms	
t_{PR}	-VCC Rising Up Time	0.1	100	-	ms	

Power on Reset Timing

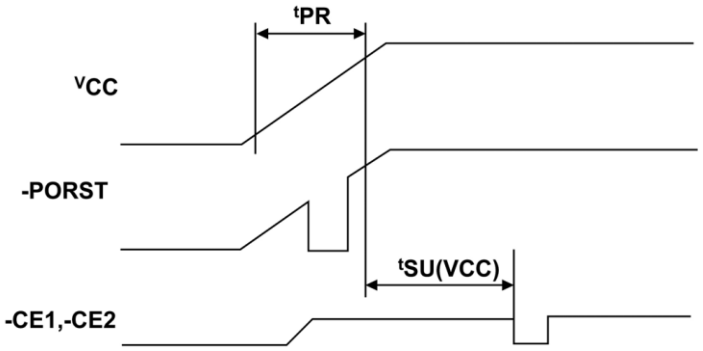

Figure 25 Timing Diagram, Power On Reset

5.11 Supported IDE Commands

EDC4000 Plus supports the commands listed in Table 44.

Table 44: IDE Commands

Command	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5h or 98h	-	-	-	-	D	-
Execute Device Diagnostic	90h	-	-	-	-	D	-
Flush Cache	E7h	-	-	-	-	Y	-
Identify Device	ECh	-	-	-	-	D	-
Idle	E3h or 97h	-	Y	-	-	D	-
Idle immediate	E1h or 95h	-	-	-	-	D	-
Read Buffer	E4h	-	-	-	-	D	-
Read DMA	C8h	-	Y	Y	Y	Y	Y
Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
Set Features	EFh	Y	-	-	-	D	-
Set Multiple Mode	C6h	-	Y	-	-	D	-
Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
SMART	B0h						
Standby	E2h or 96h	-	-	-	-	D	-
Standby Immediate	E0h or 94h	-	-	-	-	D	-
Write Buffer	E8h	-	-	-	-	D	-
Write DMA	CAh	-	Y	Y	Y	Y	Y
Write Multiple	C5h	-	Y	Y	Y	Y	Y
Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y

Defines:

FR: Feature Register

SC: Sector Count Register

SN: Sector Number Register

CY: Cylinder Registers

DH: Card/Device/Head Register

LBA: LBA Block Address Mode Supported

Y: The register contains a valid parameter for this command. For Card/Device/Head Register Y means both the CompactFlash Storage Card and head parameter are used; D – only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command description for use).

5.11.1 Check power mode – E5h or 98H

Table 45: Check power mode information

Register	7	6	5	4	3	2	1	0
Command(7)	E5h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command checks the power mode. If the CompactFlash Storage is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the compactFlash Storage Card is in idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

5.11.2 Execute Device Diagnostic – 90h

Table 46: Execute device diagnostic information

Register	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card. When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 34. Diagnostic Codes are returned in the Error Register at the end of the command.

Table 47: Diagnostic

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error

03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error
8Xh	Slave Error in True IDE Mode

5.11.3 Flush Cache- E7h

Command Code

E7h

Protocol

Non-data

Inputs

Table 48: Flush cache command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register–

DEV shall specify the selected device.

Normal Output

Table 49: Flush cache command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na

Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 50: Flush cache command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command is used by the host to request the device to flush the write cache. If there is data in write

cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

5.11.4 Identify Device – ECh

Table 51: Identify device information

Register	7	6	5	4	3	2	1	0
Command(7)	ECh							
C/D/H(6)	X	X	X	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 35. All reserved bits or words are zero. Hosts should not depend in Obsolete words in Identify Device containing 0. Table 35 specifies each filed in the data returned by the Identify Device Command. In Table 35, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 52: IDENTIFY DEVICE information

Word	Description	Value
0	General configuration bit-significant information: 15 0 = ATA device 14-8 Retired 7 1 = removable media device 6 Obsolete 5-3 Retired 2 Response incomplete 1 Retired 0 Reserved	044Ah
1	Default number of cylinders	XXXXh
2	Reserved	0000h
3	Default number of heads	00XXh
4	Obsolete	0000h
5	Obsolete	0240h

6	Default number of sectors per track	XXXXh
7-8	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)	XXXXh
9	Obsolete	0000h
10-19	Serial number (20 ASCII characters)	XXXXh
20-21	Obsolete	0002h
22	Number of ECC bytes passed on Read/Write Long Commands	0004h
23-26	Firmware revision (8 ASCII characters)	XXXXh
27-46	Model number (40 ASCII characters)	XXXXh
47	15-8 80h 7-0 00h = Reserved 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands	8001h
48	Reserved	0000h
49	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired	0F00h
50	Capabilities 15 Shell be cleared to zero 14: Shall be set to one 13-2 Reserved 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum.	0000h
51	PIO data transfer cycle timing mode	0200h
52	Obsolete	0000h
53	15-3 Reserved 2 1 = the fields reported in word 88 are valid Reserved 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid	0007h

	0 Obsolete	
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)	XXXXh
59	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command	0100h
60-61	Total number of user addressable sectors	XXXXh
62	Reserved	0000h
63	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported	0007h
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds	0078h
69-70	Reserved (for future command overlap and queuing)	0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command.	0000h
75	Queue depth 15-5 Reserved 4-0 Maximum queue depth - 1	0000h

76-79	Reserved for Serial ATA	0000h
80	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 1 = supports ATA/ATAPI-7 6 1 = supports ATA/ATAPI-6 5 1 = supports ATA/ATAPI-5 4 1 = supports ATA/ATAPI-4 3 Obsolete 2 Obsolete 1 Obsolete 0 Reserved	0000h
81	Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = See 6.17.41	0000h
82	Command set supported. 15 Obsolete 14 1 = NOP command supported 13 1 = READ BUFFER command supported 12 1 = WRITE BUFFER command supported 11 Obsolete 10 1 = Host Protected Area feature set supported 9 1 = DEVICE RESET command supported 8 1 = SERVICE interrupt supported 7 1 = release interrupt supported 6 1 = look-ahead supported 5 1 = write cache supported 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = mandatory Power Management feature set supported	7028h

	2	1 = Removable Media feature set supported	
	1	1 = Security Mode feature set supported	
	0	1 = SMART feature set supported	
83	Command sets supported.		500Ch
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = FLUSH CACHE EXT command supported	
	12	1 = mandatory FLUSH CACHE command supported	
	11	1 = Device Configuration Overlay feature set supported	
	10	1 = 48-bit Address feature set supported	
	9	1 = Automatic Acoustic Management feature set supported	
	8	1 = SET MAX security extension supported	
	7	See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6	1 = SET FEATURES subcommand required to spinup after power-up	
	5	1 = Power-Up In Standby feature set supported	
	4	1 = Removable Media Status Notification feature set supported	
	3	1 = Advanced Power Management feature set supported	
	2	1 = CFA feature set supported	
	1	1 = READ/WRITE DMA QUEUED supported	
	0	1 = DOWNLOAD MICROCODE command supported	
84	Command set/feature supported extension		4000h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report	
	11	Reserved for technical report	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64-bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Streaming feature set supported	
	3	1 = Media Card Pass Through Command feature set supported	
	2	1 = Media serial number supported	
	1	1 = SMART self-test supported	

	0 1 = SMART error logging supported	
85	Command and feature sets supported or enabled 15 Obsolete 14 1 = NOP command enabled 13 1 = READ BUFFER command enabled 12 1 = WRITE BUFFER command enabled 11 Obsolete 10 1 = Host Protected Area feature set enabled 9 1 = DEVICE RESET command enabled 8 1 = SERVICE interrupt enabled 7 1 = release interrupt enabled 6 1 = look-ahead enabled 5 1 = Write Cache enabled 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = Power Management feature set enabled 2 1 = Removable Media feature set enabled 1 1 = Security Mode feature set enabled 0 1 = SMART feature set enabled	0000h
86	Command set/feature enabled 15-14 0 = Reserved 13 1 = FLUSH CACHE EXT command supported 12 1 = FLUSH CACHE command supported 11 1 = Device Configuration Overlay supported 10 1 = 48-bit Address features set supported 9 1 = Automatic Acoustic Management feature set enabled 8 1 = SET MAX security extension enabled by SET MAX SET PASSWORD 7 See Address Offset Reserved Area Boot, INCITS TR27:2001 6 1 = SET FEATURES subcommand required to spin-up after power-up 5 1 = Power-Up In Standby feature set enabled 4 1 = Removable Media Status Notification feature set enabled 3 1 = Advanced Power Management feature set enabled 2 1 = CFA feature set enabled 1 1 = READ/WRITE DMA QUEUED command supported 0 1 = DOWNLOAD MICROCODE command supported	0000h
87	Command and feature sets supported or enabled 15 Shall be cleared to zero	4000h

	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report-	
	11	Reserved for technical report-	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64 bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Valid CONFIGURE STREAM command has been executed	
	3	1 = Media Card Pass Through Command feature set enabled	
	2	1 = Media serial number is valid	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
88	15	Reserved	001Fh
	14	1 = Ultra DMA mode 6 is selected	
		0 = Ultra DMA mode 6 is not selected	
	13	1 = Ultra DMA mode 5 is selected	
		0 = Ultra DMA mode 5 is not selected	
	12	1 = Ultra DMA mode 4 is selected	
		0 = Ultra DMA mode 4 is not selected	
	11	1 = Ultra DMA mode 3 is selected	
		0 = Ultra DMA mode 3 is not selected	
	10	1 = Ultra DMA mode 2 is selected	
		0 = Ultra DMA mode 2 is not selected	
	9	1 = Ultra DMA mode 1 is selected	
		0 = Ultra DMA mode 1 is not selected	
	8	1 = Ultra DMA mode 0 is selected	
		0 = Ultra DMA mode 0 is not selected	
	7	Reserved	
	6	1 = Ultra DMA mode 6 and below are supported	
	5	1 = Ultra DMA mode 5 and below are supported	
	4	1 = Ultra DMA mode 4 and below are supported	
	3	1 = Ultra DMA mode 3 and below are supported	
	2	1 = Ultra DMA mode 2 and below are supported	
	1	1 = Ultra DMA mode 1 and below are supported	

	0 1 = Ultra DMA mode 0 is supported	
89	Time required for security erase unit completion	0000h
90	Time required for Enhanced security erase completion	0000h
91	Current advanced power management value	0000h
92	Master Password Revision Code	0000h
93	Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset. 15 Shall be cleared to zero. 14 Shall be set to one. 13 1 = device detected CBLID- above ViH 0 = device detected CBLID- below ViL 12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows: 12 Reserved. 11 0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-. 10-9 These bits indicate how Device 1 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 8 Shall be set to one. 7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows: 7 Reserved. 6 0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected. 5 0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-. 4 0 = Device 0 did not detect the assertion of PDIAG-. 1 = Device 0 detected the assertion of PDIAG-. 3 0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics. 2-1 These bits indicate how Device 0 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown.	XXXXh

	0 Shall be set to one.	
94	15-8 Vendor's recommended acoustic management value. 7-0 Current automatic acoustic management value.	0000h
95	Stream Minimum Request Size	0000h
96	Streaming Transfer Time - DMA	0000h
97	Streaming Access Latency - DMA and PIO	0000h
98-99	Streaming Performance Granularity	0000h
100-103	Maximum user LBA for 48-bit Address feature set.	0000h
104	Streaming Transfer Time - PIO	0000h
105	Reserved	0000h
106	Physical sector size / Logical Sector Size 15 Shall be cleared to zero 14 Shall be set to one 13 1 = Device has multiple logical sectors per physical sector. 12 1= Device Logical Sector Longer than 256 Words 11-4 Reserved 3-0 2 logical sectors per physical sector	0000h
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds	0000h
108	15-12 NAA (3:0) 11-0 IEEE OUI (23:12)	0000h
109	15-4 IEEE OUI (11:0) 3-0 Unique ID (35:32)	0000h
110	15-0 Unique ID (31:16)	0000h
111	15-0 Unique ID (15:0)	0000h
112-115	Reserved for world wide name extension to 128 bits	0000h
116	Reserved for technical report-	0000h
117-118	Words per Logical Sector	0000h

119-120	Reserved	0000h
121-126	Reserved	0000h
127	Removable Media Status Notification feature set support 15-2 Reserved 1-0 00 = Removable Media Status Notification feature set not supported 01 = Removable Media Status Notification feature supported 10 = Reserved 11 = Reserved	0000h
128	Security Status 15-9 Reserved 8 Security level 0 = high, 1 = Maximum 7-6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 1 = Security frozen 2 1 = Security locked 1 1 = Security enabled 0 1 = Security supported	0000h
129-159	Vendor specific	0000h
160	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma	81F4h
161	Reserved	0000h
162	Key management schemes supported	0000h
163	CF Advanced True IDE Timing Mode Capability and Setting	0092h
164	CF Advanced PCMCIA I/O and Memory Timing Mode Capability and Setting 80ns cycle in memory and I/O mode	0000h
161-175	Reserved for assignment by the CompactFlash™ Association	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15-8 Checksum 7-0 Signature	0000h

5.11.5 Idle – E3h or 97h

Table 53: Idle information

Register	7	6	5	4	3	2	1	0
Command(7)	E3h or 97h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Timer Count (5 msec increments)							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

5.11.6 Idle immediate –E1h or 95h

Table 54: Idle immediate information

Register	7	6	5	4	3	2	1	0
Command(7)	E1h or 95h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

5.11.7 Read Buffer – E4h

Table 55: Read buffer information

Register	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							

Sector Count(2)	X
Feature(1)	X

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

5.11.8 Read DMA – C8h

Table 56: Read DMA information

Register	7	6	5	4	3	2	1	0
Command(7)	C8h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16							
Cylinder Low(4)	Cylinder Low (LBA 15-8							
Sector Number(3)	Sector Numbe(LBA 7-0							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 request 256 sectors. The transfer begins at he sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, cleat BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 & sector –count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector number of the sector where the occurred. The amount of data transferred is indeterminate. When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

5.11.9 Read Sector(s) – 20h or 21h

Table 57: Read sector information

Register	7	6	5	4	3	2	1	0
Command(7)	20h or 21h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							

Cylinder Low(4)	Cylinder Low (LBA 15-8)
Sector Number(3)	Sector Number (LBA 7-0)
Sector Count(2)	Sector Count
Feature(1)	X

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2where the error occurred. The flawed data is pending in the sector buffer.

5.11.10 Read Verify Sector(s) – 40h or 41h

Table 58: Read verify sector information

Register	7	6	5	4	3	2	1	0
Command(7)	40h or 41h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

5.11.11 Set Features – EFh

Table 59: Set feature information

Register	7	6	5	4	3	2	1	0
Command(7)	EFh							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							

Cylinder Low(4)	X
Sector Number(3)	X
Sector Count(2)	Config
Feature(1)	Feature

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CompactFlash Storage Card shall return command aborted. Table 37: Feature Supported defines all features that are supported.

Table 60: Feature Supported

Command Name	Code	Sub Command
Set Transfer Mode	EFh	03h
Disable Read Look-ahead feature	EFh	55h
Enable write cache	EFh	02h
Disable reverting to power-on defaults	EFh	66h
Disable write cache	EFh	82h
Enable reverting to power-on defaults	EFh	CCh

5.11.12 Set Multiple Mode – C6h

Table 61: Set multiple mode information

Register	7	6	5	4	3	2	1	0
Command(7)	C6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command enables the CompactFlash Storage Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash Storage Card sets BSY to 1 and checks the Sector Count Register. If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled

by a Set Feature command) software reset, the default mode is Read and Write multiple disabled.

5.11.13 Set Sleep Mode –E6h or 99h

Table 62: Set sleep mode information

Register	7	6	5	4	3	2	1	0
Command(7)	E6h or 99h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

5.11.14 Standby –E2h or 96h

Table 63: Standby information

Register	7	6	5	4	3	2	1	0
Command(7)	E2h or 96h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

5.11.15 Standby Immediate –E0h or 94h

Table 64: Standby immediate information

Register	7	6	5	4	3	2	1	0
Command(7)	E0h or 94h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							

Sector Number(3)	X
Sector Count(2)	X
Feature(1)	X

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

5.11.16 Write Buffer – E8h

Table 65: Write buffer information

Register	7	6	5	4	3	2	1	0
Command(7)	E8h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

5.11.17 Write DMA – CAh

Table 66: Write DMA information

Register	7	6	5	4	3	2	1	0
Command(7)	CAh							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low(LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512*sector count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecovertable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The amount of data transferred is indeterminate. When a write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

5.11.18 Write Multiple- C5h

Command Code

C5h

Protocol

PIO data-out

Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 67: Write multiple command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

Normal Output

Table 68: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 69: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

N = Remainder (sector count / block count).

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the

attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

5.11.19Write Sector(s) – 30h or 31h

Table 70: Write sector information

Register	7	6	5	4	3	2	1	0
Command(7)	30h or 31h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

5.11.20 SMART

Individual SMART commands are identified by the value placed in the Feature register.

Table 71: SMART Feature register values

Value	Command
D0h	SMART Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

SMART Read Data

Command Code

B0h with a Feature register value of D0h

Feature Set

Smart Feature Set

- Operation when the SMART feature set is implemented.

Protocol

PIO data-in

Inputs

Table 72: SMART command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 73: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one. SMART enabled.

Description

This command returns the Device SMART data structure to the host.

Table 74: SMART data structure

BYTE	Description
0-1	Revision code
2-361	Vendor specific
362	Off-line data collection status
364-365	Self-test execution status byte
366	Total time in seconds to complete off-line data collection activity
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability
371	Vendor specific
372	Short self-test routine recommended polling time
373	Extended self-test routine recommended polling time
374	Conveyance self-test routine recommended polling time
375-385	Reserved
386-395	Firmware Version/Date Code
396-397	Number of initial invalid block(396=MSB, 397 = LSB)
398-399	Number of run time bad block(398=MSB, 399=LSB)

400	Number of spare block
401-402	Erase count(401=MSB, 402=LSB)
511	Checksum

SMART ENABLE OPERATIONS

Command Code

B0h with a Feature register value of D8h

Feature Set

Smart Feature Set

Protocol

Non-data

Inputs

Table 75: SMART Enable command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 76: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one.

Description

This command enables access to all SMART capabilities within device.

SMART DISABLE OPERATIONS

Command Code

B0h with a Feature register value of D9h

Feature Set

Smart Feature Set

Protocol

Non-data

Inputs

Table 77: SMART DISABLE Command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 78: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one. SMART enabled.

Description

This command disables all SMART capabilities within device.

5.12 Device Parameters

EDC4000 Plus device parameters are listed in Table 79.

Table 79: Device parameters

Capacity	Cylinders	Heads	Sectors	LBA
512MB	991	16	63	998928
1GB	1966	16	63	1981728
2GB	3900	16	63	3931200
4GB	7785	16	63	7847280
8GB	15538	16	63	15662304
16GB	16383	16	63	31293360
32GB	16383	16	63	62537328

InnoDisk Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	D	**E**	**X**	**H**	**-**	**0**	**4**	**G**	**D**	**5**	**2**	**W**	**X**	**D**	**S**	**-**	**X**
Description	Disk	EDC4000 Plus			-	Capacity			Category			Operation Temp.	Internal Control	-	flash		Customized Code

Definition	
Code 1st (Disk)	**Code 13th (Internal Control Code)**
D : Disk	1: 1st PCB version, default setting
Code 2nd ~ 4th (Form Factor)	
EXH：EDC4000 Plus	**Code 14th (Channel of data transfer)**
E4S：44-pin EDC,Write Protect	S: Single Channel
E4P: 44-pin EDC, Horizontal	
Code 6th ~8th (Capacity)	D: Dual Channel
128: 128MB	
256: 256MB	**Code 15th**
512: 512MB	S: Samsung flash
01G: 1GB	T: Micron flash
02G: 2GB	**Code 17th**
04G：4GB	Customized code
08G：8GB	
16G：16GB	
32G：32GB	
Code 9th ~ 11th (Series)	
D51：EDC4000 Plus	
Code 12th (Operation Temperature)	
C: Standard Grade(0℃ ~ +70 ℃)	
W：Industrial Grade (-40℃ ~ +85 ℃)	