

RoHS Compliant

512MB DDR SDRAM UDIMM

Product Specifications

May 22, 2014

Version 1.1



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General Description

Apacer **77.G1736.44G** is 64M x 64 Double Data Rate SDRAM high density memory modules based on first generation of 512Mb DDR SDRAM respectively. It consists of 8 pieces 64M x8 bit with 4 banks Double Data Rate SDRAMs in 66 pin TSOP-II (400mil) packages mounted on a 184pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. This product is Dual In-line Memory Modules and intended for mounting into 184 pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
77.G1736.44G	3.2 GB/sec	400 Mbps	200 MHz	CL3

Density	Organization	Component	Rank
512MB	64M x 64	64M x8*8	1

Key Parameters

MT/s	DDR-266	DDR-266	DDR-333	DDR-400	Unit
Grade	-CL2	-CL2.5	-CL2.5	-CL3	
tCK (min)	7.5	7.5	6	5	ns
CAS latency	2	2.5	2.5	3	tCK
tRC	9	9	10	11	tCK
tRAS	6	6	7	8	tCK
CL-tRCD-tRP	2-3-3	2.5-3-3	2.5-3-3	3-3-3	tCK

Specifications:

- ◆ Power supply V_{DD} : 2.6V +/-0.1V
- ◆ MRS cycle with address key programs
- ◆ CAS Latency (Access from column address) : 2.5, 3
- ◆ Burst length : 2, 4, 8
- ◆ Data scramble : Sequential & Interleave
- ◆ Serial presence detect with EEPROM
- ◆ Differential clock input
- ◆ Compliance With RoHS
- ◆ Compliance With CE
- ◆ SSTL_2-compatible
- ◆ Auto Refresh and self Refresh Modes 64ms, 8192-cycle refresh
- ◆ Operating Temperature Rang : Commercial $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$

Pin Assignments

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	24	DQ17	47	DQS8*	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	Vss	26	Vss	49	CB2*	72	DQ48
4	DQ1	27	A9	50	Vss	73	DQ49
5	DQS0	28	DQ18	51	CB3*	74	Vss
6	DQ2	29	A7	52	BA1	75	/CK2
7	VDD	30	VDDQ	53	DQ32	76	CK2
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ
9	NC	32	A5	55	DQ33	78	DQS6
10	NC	33	DQ24	56	DQS4	79	DQ50
11	Vss	34	Vss	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	Vss	81	Vss
13	DQ9	36	DQS3	59	BA0	82	VDDID
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	CK1	39	DQ26	62	VDDQ	85	VDD
17	/CK1	40	DQ27	63	/WE	86	DQS7
18	Vss	41	A2	64	DQ41	87	DQ58
19	DQ10	42	Vss	65	/CAS	88	DQ59
20	DQ11	43	A1	66	Vss	89	Vss
21	CKE0	44	CB0*	67	DQS5	90	NC
22	VDDQ	45	CB1*	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
93	Vss	116	Vss	139	Vss	162	DQ47
94	DQ4	117	DQ21	140	DM8*	163	NC
95	DQ5	118	A11	141	A10	164	VDDQ
96	VDDQ	119	DM2	142	CB6*	165	DQ52
97	DM0	120	VDD	143	VDDQ	166	DQ53
98	DQ6	121	DQ22	144	CB7	167	NC
99	DQ7	122	A8	145	Vss	168	VDD
100	Vss	123	DQ23	146	DQ36	169	DM6
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	A13	126	DQ28	149	DM4	172	VDDQ
104	VDDQ	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDDQ	151	DQ39	174	DQ60
106	DQ13	129	DM3	152	Vss	175	DQ61
107	DM1	130	A3	153	DQ44	176	Vss
108	VDD	131	DQ30	154	/RAS	177	DM7
109	DQ14	132	Vss	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDDQ	179	DQ63
111	CKE1	134	CB4*	157	/CS0	180	VDDQ
112	VDDQ	135	CB5*	158	/CS1*	181	SA0
113	BA2*	136	VDDQ	159	DM5	182	SA1
114	DQ20	137	CK0	160	Vss	183	SA2
115	A12	138	/CK0	161	DQ46	184	VDDSPD

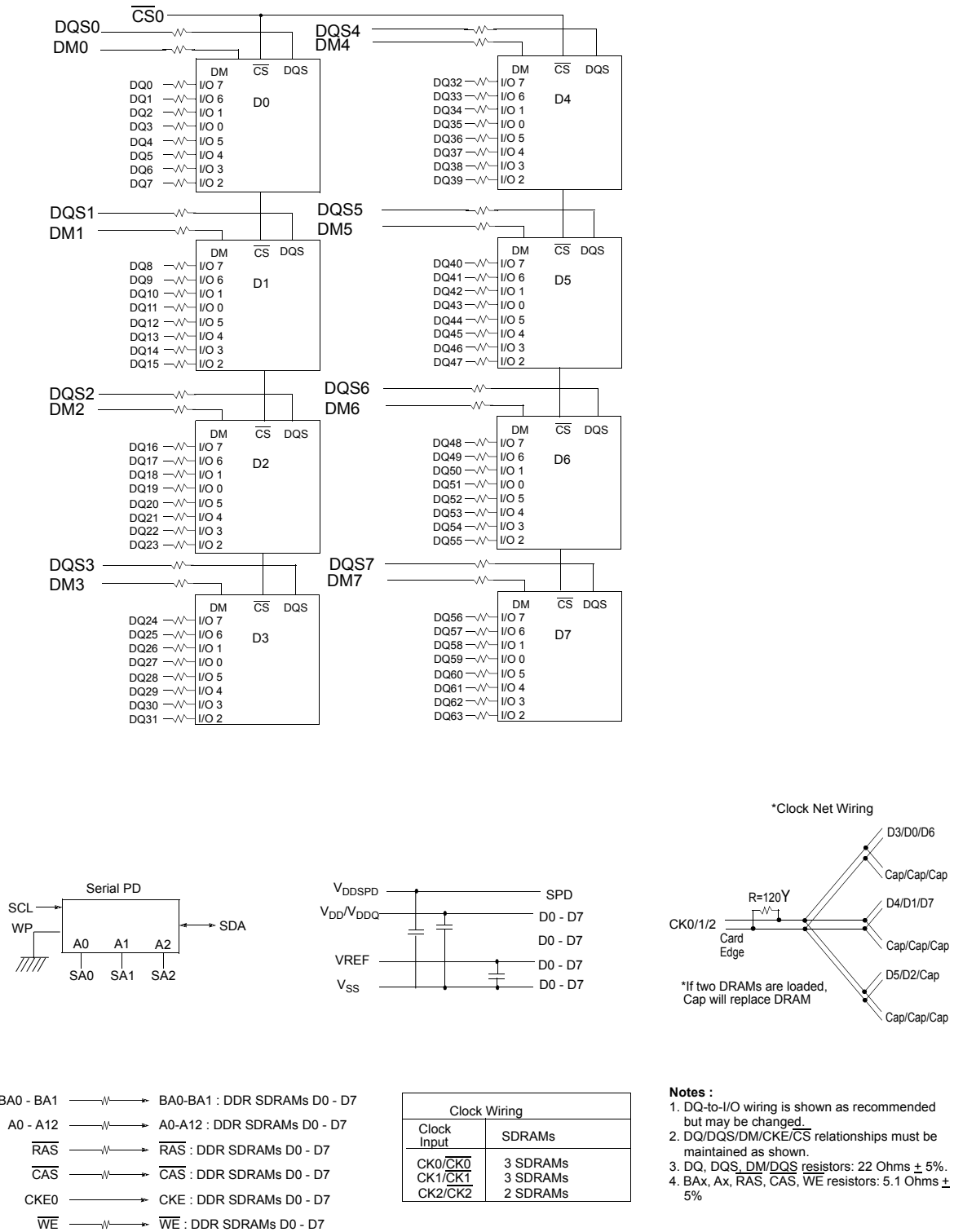
Notes:

*These pins are not used in this module.

Pin Descriptions

Pin Name	Description
Ax	SDRAM address bus
BAx	SDRAM bank select
/RAS	SDRAM row address strobe
/CAS	SDRAM column address strobe
/WE	SDRAM write enable
/CSx	DIMM Rank Select Lines
CKEx	SDRAM clock enable lines
DQx	DIMM memory data bus
DQSx	SDRAM data strobes(positive line of differential pair)
DMx	SDRAM data masks high data strobes(x8-based X72 DIMMs)
CKx	SDRAM clocks(positive line of differential pair)
/CKx	SDRAM clocks(negative line of differential pair)
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data line for EEPROM
SAX	I2C slave address select for EEPROM
VDD	SDRAM core power supply
VDDQ	SDRAM I/O Driver power supply
VREF	Power supply reference
VSS	Power supply return(ground)
VDDSPD	Serial EEPROM positive power supply
VDDID	VDD identification flag
NC	Spare pins(no connect)

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Description	Units
Supply Voltage Relative to VSS	V _{DD}	- 1.0 V ~ 3.6 V	V
Supply Voltage Relative to VSS	V _{DDQ}	- 1.0 V ~ 3.6 V	V
VREF and Inputs Voltage Relative to VSS	V _{IN} , V _{OUT}	- 0.5 V ~ 3.6 V	V
Storage Temperature	TSTG	-55 to +100	°C

Notes:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TA	Operating Temperature Range	0 to 70	°C	

Operating Conditions

Recommended DC Operating Conditions - DDR (2.6V $\pm$ 0.1V) operation

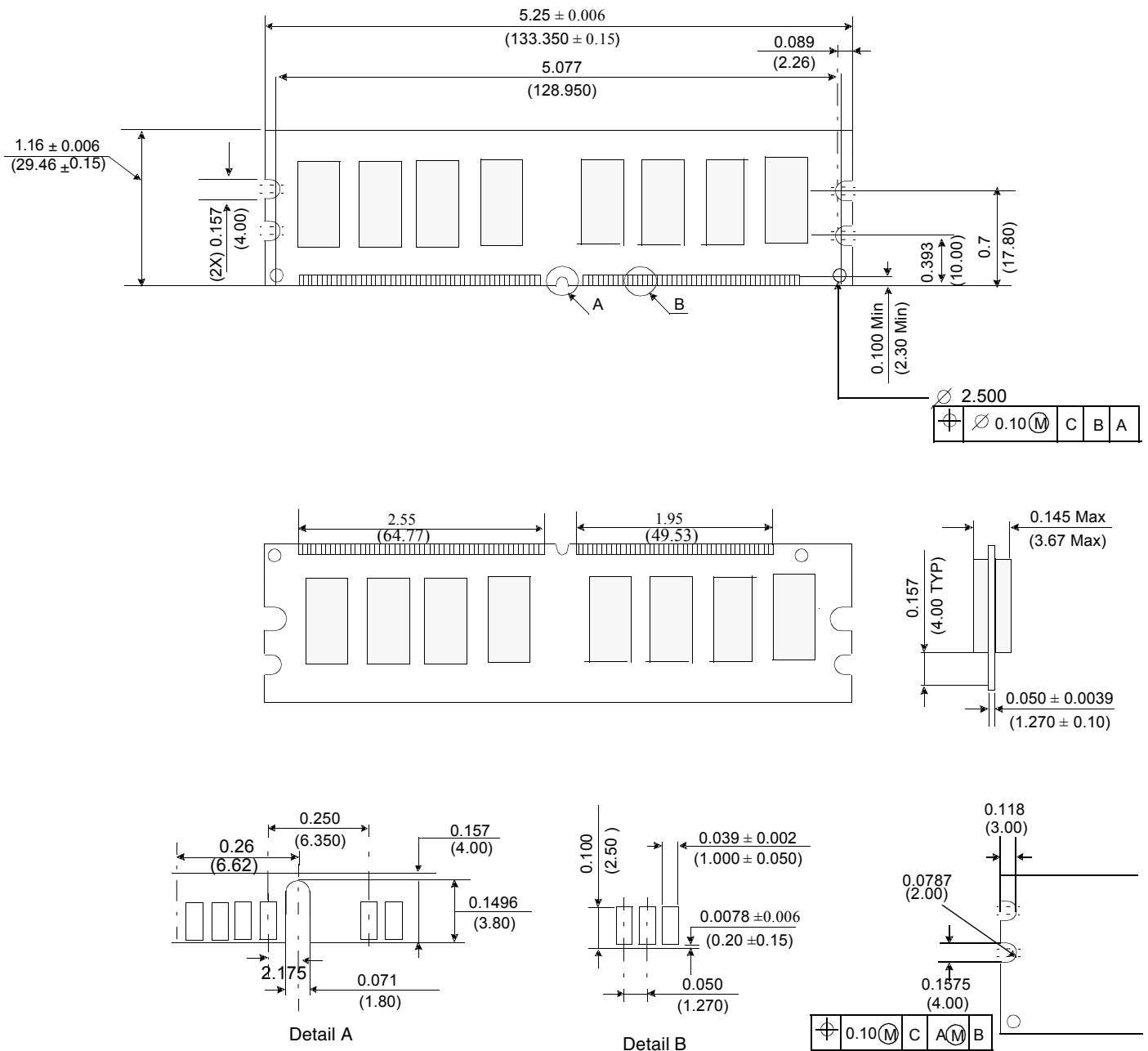
Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
V _{DD}	Supply Voltage	2.5	2.6	2.7	V
V _{DDQ}	Supply Voltage for Output	2.5	2.6	2.7	V

Notes:

1. V_{REF} is expected to be equal to 0.5 x V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.

Mechanical Drawing

Units : Inches (Millimeters)



Tolerances : ± 0.005 (0.13) unless otherwise specified.
The used device is 64Mx8 SDRAM, TSOP.

Revision History

Revision	Date	Description	Remark
0.9	08/28/2012	Official release	
1.0	08/29/2012	release	
1.1	07/23/2013	Changed headquarters address	

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