

RoHS Recast Compliant

ATA Disk Module 4

Specifications for Mini ADM-M (44P/270D)

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Version 1.2



Apacer Technology Inc.

4th Fl., 75 Hsin Tai Wu Rd., Sec.1, Xizhi, New Taipei City, Taiwan 221

Tel: +886-2-2698-2888 Fax: +886-2-2698-2889

www.apacer.com

Features:

- **Standard ATA/IDE bus interface**
 - ATA command set compatible
 - ATA operating mode supports up to:
 - PIO Mode-4
 - Multiword DMA Mode-2
 - Ultra DMA Mode-6
- **Connector type**
 - 44-pin female connector
- **Power consumption (typical)**
 - Supply voltage: 3.3V & 5V
 - Active mode: 205 mA
 - Idle mode: 10 mA
- **Performance***
 - Sustained read: 85 MB/sec
 - Sustained write: 28 MB/sec
- **Capacity**
 - Standard:
 - 4, 8, 16, 32, 64, 128 GB
- **NAND Flash Type: MLC**
- **Temperature ranges**
 - Operation: 0°C to 70°C
 - Storage: -40°C to 100°C
- **Flash management**
 - Intelligent endurance design
 - Advanced wear-leveling algorithms*
 - S.M.A.R.T. technology*
 - Built-in hardware ECC*
 - Power Failure Management
 - Enhanced security level
 - ATA Secure Erase*
- **RoHS compliant**
- **Form factor**
 - Mini ATA disk module
- **Dimensions**
 - 45.00 x 32.60 x 6.80**, unit: mm

*Performance and power consumption may vary from flash configurations or host system settings.

** Including the height of ATA connector

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1. General Description

Apacer's ATA-Disk Module (ADM) is a high-performance, embedded flash drive designed to replace the conventional IDE hard disk drive. The ADMs can be plugged into a standard IDE connector commonly found in desktops, IT-STB, industrial PCs and thin client systems. Apacer's ADM SSD has a built-in microcontroller with file management firmware that communicates with the ATA standard interfaces. No additional or proprietary host software is required.

Well suited for embedded flash storage applications by offering new and expanded functionalities as well as more cost-effective designs, better performance and increased reliability, ADM is designed to work at either 5 or 3.3 Volts, supports the standard ATA/IDE protocol for up to PIO Mode-4, Multiword DMA Mode-2 and Ultra DMA Mode-6 interfaces, and uses the standard ATA driver complying with all major operating systems such as Microsoft's Windows series, Apple's Mac OS family, and Unix variants.

Featuring technologies as Advanced Wear-leveling algorithms, S.M.A.R.T, Flash Block Management, Power Failure Management, Wear Leveling and ATA Secure Erase, Apacer's ADM assures users of a versatile device on data storage.

2. Functional Block

The ATA-Disk Module (ADM) includes the ATA controller and flash media, as well as the ATA standard interface. Figure 2-1 shows the functional block diagram.

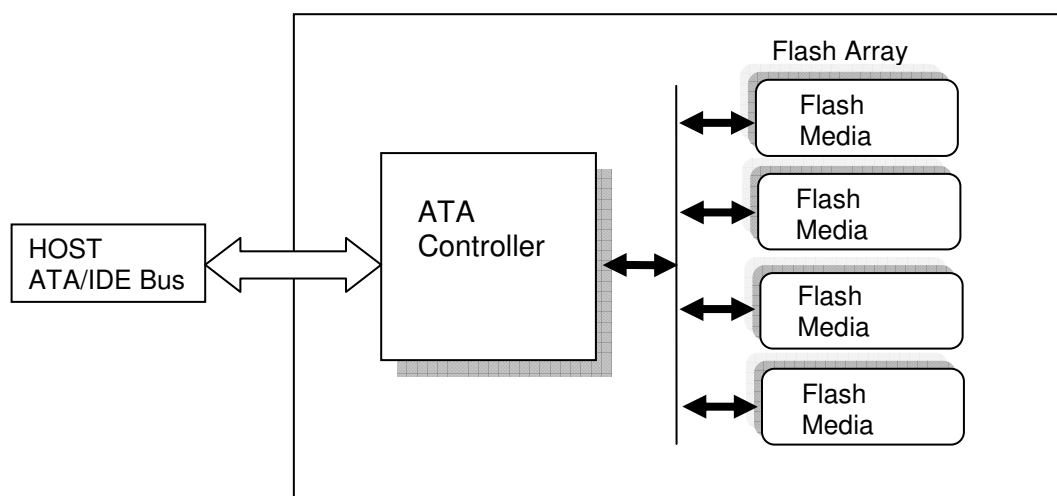


Figure 2-1: Functional block diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 44-pin configuration. A “#” suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1: Pin assignments for the 44-pin configuration

Pin No.	Signal Name	Pin Type	I/O Type*	Pin No.	Signal Name	Pin Type	I/O Type
1	RESET#	I	I2U	2	GND	-	Ground
3	D7	I/O	I1Z, O2	4	D8	I/O	I1Z, O2
5	D6	I/O	I1Z, O2	6	D9	I/O	I1Z, O2
7	D5	I/O	I1Z, O2	8	D10	I/O	I1Z, O2
9	D4	I/O	I1Z, O2	10	D11	I/O	I1Z, O2
11	D3	I/O	I1Z, O2	12	D12	I/O	I1Z, O2
13	D2	I/O	I1Z, O2	14	D13	I/O	I1Z, O2
15	D1	I/O	I1Z, O2	16	D14	I/O	I1Z, O2
17	D0	I/O	I1Z, O2	18	D15	I/O	I1Z, O2
19	GND	-	Ground	20	NC	-	-
21	DMARQ#	O	O1	22	GND		Ground
23	IOWR# STOP	I	I2Z	24	GND	-	Ground
25	IORD# HDMARDY# HSTROBE#	I	I2Z	26	GND	-	Ground
27	IORDY DDMARDY# DSTROBE	O	O1	28	NC/CSEL	I	I1U
29	DMACK#	I	I2U	30	NC/WP#*	-/I	-/I1U
31	INTRQ	O	O1	32	IOCS16#	O	O2
33	A1	I	I1Z	34	PDIAG#	I/O	I1U, O1
35	A0	I	I1Z	36	A2	I	I1Z
37	CS1FX#	I	I2Z	38	CS3FX#	I	I2Z
39	DASP#	I/O	I1U, O6	40	GND	-	Ground
41	VDD	-	Power	42	VDD	-	Power
43	GND	-	Ground	44	NC	-	-

*Pin 30 is selectable as NC or WP# through a zero ohm resistor jumper. Default is NC. Note that pin 30 is a GND pin on standard ATA interface. This pin could be redesigned for host to control the write protect function on ADM

4. Product Specifications

4.1 Capacity Specification

Capacity of I ATA-Disk Module (ADM) product series is listed as out-of-box and unformatted.

Table 4-1: Capacity specifications

Capacity	Total bytes	Cylinders	Heads	Sectors	Max LBA
4 GB	3,917,168,640	7937	16	63	7,650,720
8 GB	7,682,605,056	15504	16	63	15,005,088
16 GB	15,521,009,664	16383	16	63	30,314,472
32 GB	31,042,019,328	16383	16	63	60,628,944
64 GB	62,084,038,656	16383	16	63	121,257,888
128 GB	124,168,077,312	16383	16	63	242,515,716

*Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

**Display of total bytes varies from file systems.

***Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance Specification

Table 4-2: Performance specifications

Capacity	4 GB	8 GB	16 GB	32 GB	64 GB	128 GB
Performance						
Sustained read (MB/s)	41	41	50	80	80	80
Sustained write (MB/s)	6	6	10	17	26	20

*Results may differ from various flash configurations and platforms.

4.3 Environmental Specification

Environmental specification of the ATA-Disk Module (ADM) product family follows the MIL-STD-810F standard.

Table 4-5: Environmental specifications

Environment	Specification
Temperature	Operation 0°C to 70°C
	Storage -40°C to 100°C
Humidity	5% to 95% RH (Non-condensing)
Vibration (Non-Operating)	Sine wave : 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operating)	Half sine wave, Peak acceleration 1500 G (X, Y, Z ; All 6 axes)

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in this device. The measurement assumes that device failure rate can be generated by the sum of failure rates in each component and a steady state failure rate can be predicated as equal to or greater than 2.55×10^6 hours.

Notes about the MTBF:

The MTBF is predicated and calculated based on “Bellcore Analysis Method 1”.

$$\lambda_{ss} = \pi_E \sum_{i=1}^m (Ni \lambda_{SSi})$$

m : number of component types

λ_{ss} : device failure rate at steady state

Ni : quantity of i type component

λ_{SSi} : failure rate for i type component at steady state

π_E : device environment factor

5. Flash Management

5.1 Advanced wear-leveling algorithms

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

5.2 Built-in hardware ECC

The ATA-Disk Module uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to 12 random bits of error per 512-Byte sector or 24 random bits of error per 1K-Byte sector. High performance is fulfilled through hardware-based error detection and correction.

5.3 Flash Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.4 Power Failure Recovery

Power Failure Recovery plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

6. Software Interface

6.1 Command Set

Table 6-1: Command set (1 of 2)

Command	Code	FR ¹	SC ²	SN ³	CY ⁴	DH ⁵	LBA ⁶
Check-Power-Mode	E5H or 98H	-	-	-	-	D ⁸	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
Flush-Cache	E7H	-	-	-	-	D	-
Format Track	50H	-	Y ⁷	-	Y	Y ⁸	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Request-Sense	03H	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y ⁷	-	-	-	D	-
SMART	B0H	Y	Y	Y	Y	D	
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Translate-Sector	87H	-	Y	Y	Y	Y	Y

Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-Without-Erase	CDH	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector-Without-Erase	38H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

1. FR – Features register
2. SC – Sector Count register
3. SN – Sector Number register
4. CY – Cylinder registers
5. DH – Drive/Head register
6. LBA – Logical Block Address mode supported (see command descriptions for use)
7. Y – The register contains a valid parameter for this command
8. For the Drive/Head register:

Y means both the ATA-Disk Module and Head parameters are used

D means only the ATA-Disk Module parameter is valid and not the Head parameter

6.2 S.M.A.R.T.

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and attributes parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our SMART feature that complies with the ATA/ATAPI-7 specifications. Based on the SFF-8035i Rev. 2.0 specifications, SMART Attribute IDs shall include Initial bad block count, Bad block count, Spare block count, Maximum erase count, Average erase count and Power cycle. When the SMART Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

6.3. ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

7. Electrical Specification

Caution: Absolute Maximum Stress Ratings – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1: Operating range

Ambient Temperature	3.3V	5V
0°C to +70°C	3.135-3.465V	4.75-5.25V

Table 7-2: Absolute maximum power pin stress ratings

Parameter	Symbol	Voltage	Conditions
Input Power	V_{DDQ}	3.3 V	-0.3V min to 4.0V max
		5 V	-0.3V min. to 6.5V max.
	$V_{DD(core)}$ and $V_{DD(I/O)}$	3.3 V	-0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}	-	-	-0.5V min to $V_{DD} + 0.5V$ max

Table 7-3: Recommended system power-up timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-READY}^*$	Power-up to Ready Operation	200	2000	ms
$T_{PU-WRITE}^*$	Power-up to Write Operation	200	2000	ms

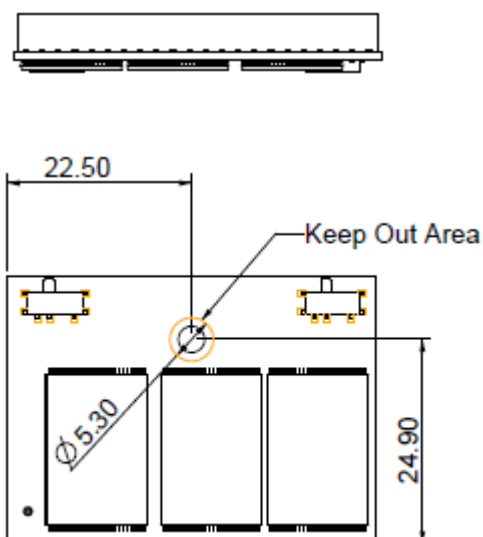
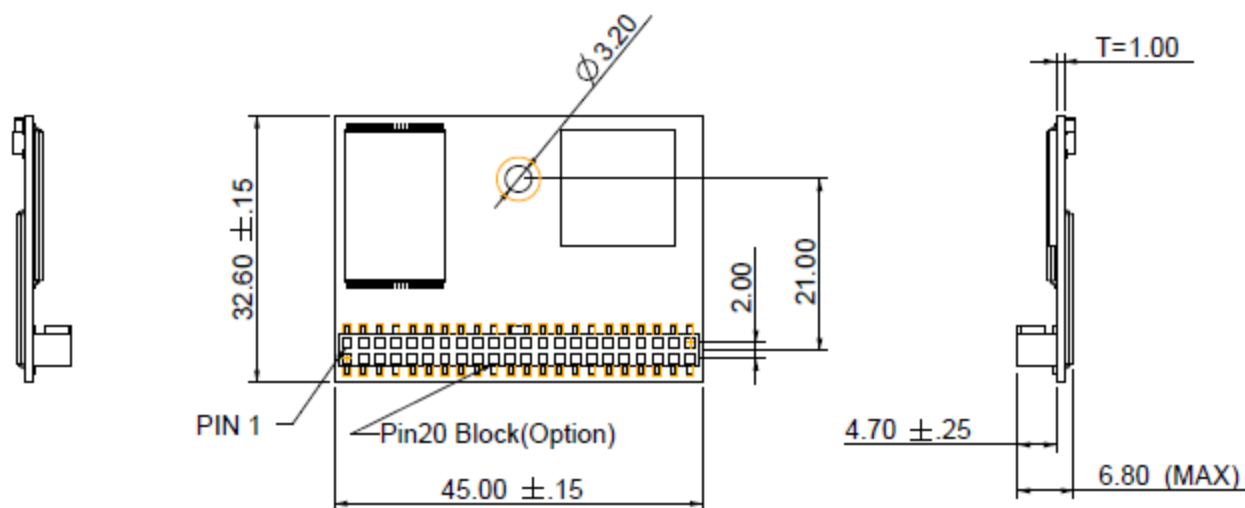
*This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 7-4: Power consumptions

Capacity	4 GB	8 GB	16 GB	32 GB	64 GB	128 GB
States						
Operating (mA)	155	155	177	177	195	205
Idle (mA)	10	10	10	10	10	10

*Results may differ from various flash configurations and platforms.

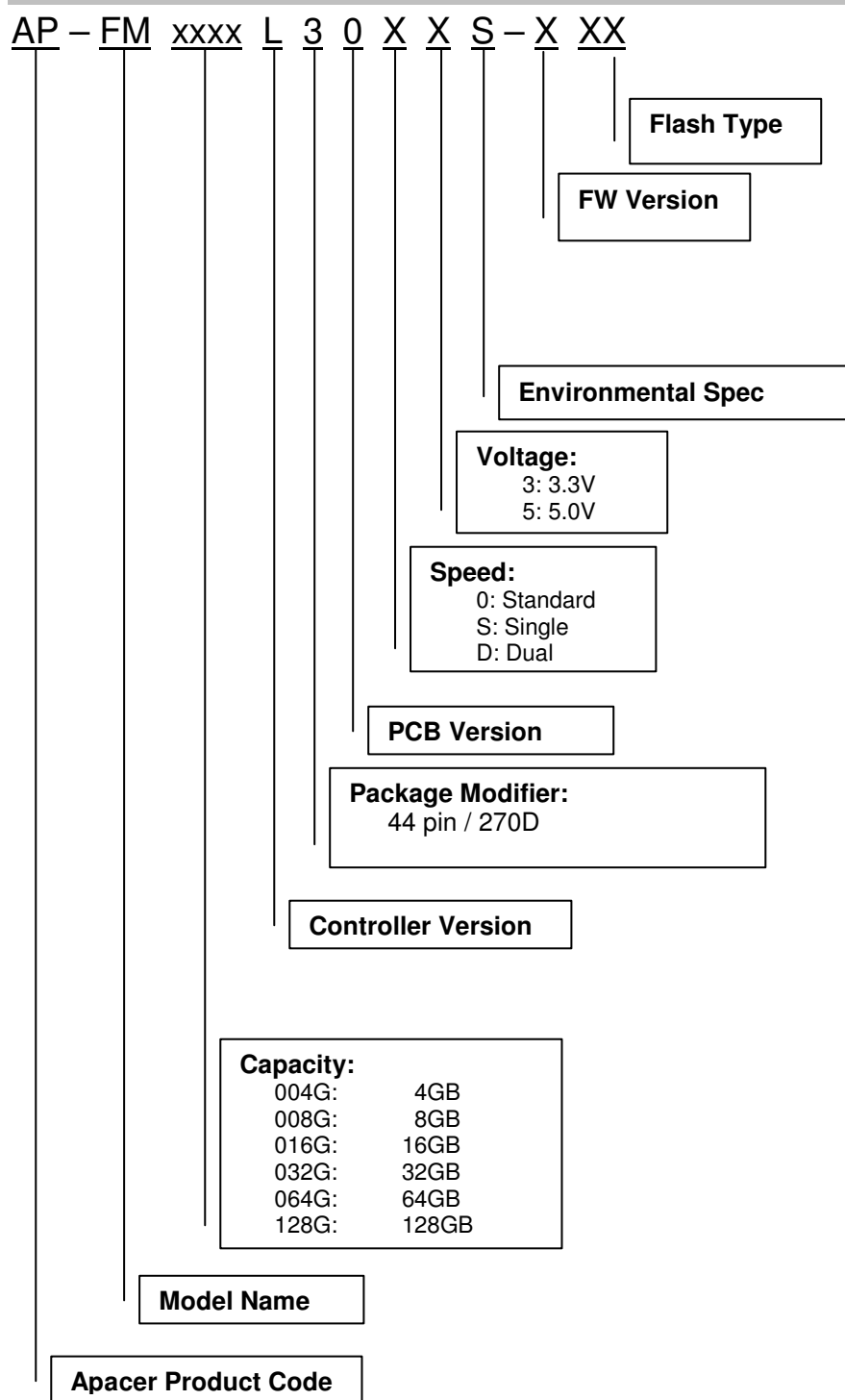
8.1 Dimension – Mini ADM



Unit: mm
Tolerance: ± 0.2 mm

9. Product Ordering Information

9.1 Product Code Designations



9.2 Valid Combinations

9.2.1 Standard MLC

Standard Capacity	P/N (3.3V)	P/N (5V)
4GB	AP-FM004GL3003S-DCM	AP-FM004GL3005S-DCM
8GB	AP-FM008GL3003S-DCM	AP-FM008GL3005S-DCM
16GB	AP-FM016GL3003S-DCM	AP-FM016GL3005S-DCM
32GB	AP-FM032GL3003S-DCM	AP-FM032GL3005S-DCM
64GB	AP-FM064GL3003S-DCM	AP-FM064GL3005S-DCM
128GB	AP-FM128GL3003S-DCM	AP-FM128GL3005S-DCM

Revision History

Revision	Date	Description	Remark
1.0	05/06/2011	Official release	
1.1	08/09/2012	Updated mechanical drawing	
1.2	12/13/2012	Updated performance, power consumption and Product Ordering Information due to change in flash configurations	

Global Presence

Taiwan (Headquarters)	Apacer Technology Inc. 4 th Fl, 75 Hsin Tai Wu Rd., Sec.1 Xizhi, New Taipei City Taiwan 221 R.O.C. Tel: +886-2-2698-2888 Fax: +886-2-2698-2889 amtsales@apacer.com
U.S.A.	Apacer Memory America, Inc. 386 Fairview Way, Suite102, Milpitas, CA 95035 Tel: 1-408-518-8699 Fax: 1-408-935-9611 sa@apacerus.com
Japan	Apacer Technology Corp. 5F, Matsura Bldg., Shiba, Minato-Ku Tokyo, 105-0014, Japan Tel: 81-3-5419-2668 Fax: 81-3-5419-0018 jpservices@apacer.com
Europe	Apacer Technology B.V. Science Park Eindhoven 5051 5692 EB Son, The Netherlands Tel: 31-40-267-0000 Fax: 31-40-267-0000#6199 sales@apacer.nl
China	Apacer Electronic (Shanghai) Co., Ltd 1301, No.251,Xiaomugiao Road, Shanghai, 200032, China Tel: 86-21-5529-0222 Fax: 86-21-5206-6939 sales@apacer.com.cn
India	Apacer Technologies Pvt Ltd, # 535, 1st Floor, 8th cross, JP Nagar 3rd Phase, Bangalore – 560078, India Tel: 91-80-4152-9061 sales_india@apacer.com