

PXI-2022 16-bit, 250KS/s, 16 Channels Simultaneous Sampling Card

Features

- Supports 3.3V and 5V PCI signaling
- PXI specification Rev 2.2 compliant
- 16-CH differential analog inputs
- Bipolar analog input
- Programmable gains of x1, x4
- Scatter gather DMA transfer for AI continuously data acquisition
- 4-CH TTL digital input/output
- 3U EuroCard form factor
- 2-CH 32-bit general purpose timer/counters
- Digital triggering
- Fully auto calibration
- Multiple cards synchronization through PXI trigger bus
- Onboard 8K sample(16K bytes) memory for data storage

Introduction

ADLINK's PXI-2022 is a simultaneous-sampling multi-function DAQ card to meet a wide range of application requirements. The device can simultaneously sample 16 AI channels with differential input configurations in order to achieve maximum noise elimination. If more analog input or output channels are required, multiple cards can be synchronized through the PXI Trigger bus. The PXI-2022 features digital triggering, 4-CH programmable digital I/O lines, and 2-CH 32-bit general-purpose timer/counters. The auto-calibration functions adjust the gain and offset to within specified accuracies such that you do not have to adjust trim pots to calibrate the cards.

Operating System

Windows Vista/XP/2000/2003

Specifications

Analog Input

Model Name	PXI-2022
A/D converter	ADI AD7685
Resolution	16 bits
Number of Channels	16 differential channels
Input Impedance	1 GΩ/pF
Input Coupling	DC
Bipolar Input Signal Range	±10 V, ±2.5 V
Programmable gain	1, 4
Overvoltage Protection	Power on: ±30 V continuous Power off: ±30 V continuous
Max Sampling Rate	250 KS/s
ADC Resolution	16 bits, 1 in 65535
Data FIFO Size	8K sample (16 bytes)
DNL (gain =1)	± 0.8 LSB
INL (gain =1)	± 1.5 LSB (typical), ± 3.0 LSB (MAX)
Offset Error (gain =1)	0.6mV (typical)
Gain Error (gain =1)	0.05% of input
Offset Temperature Drift	0.1 mV/°C (typical)
-3dB Bandwidth	gain =1 : 1 MHz gain = 4 : 700 KHz
System noise	gain =1 : 0.5 mVrms gain =4 : 0.2 mVrms
CMRR*(2)	gain =1 : 80 dB gain =4 : 80 dB
Spurious-free dynamic range (SFDR)	87 dB
Signal-to-noise and distortion ratio (SINAD)	82 dB
Total harmonic distortion (THD)	-85 dB
Signal-to-noise ration (SNR)	84 dB
Data Transfer	Scatter-gather DMA, Polling Mode

Triggers

Model Name	PXI-2022
Trigger Sources	(1)Software (2)AFI [0..7] (3)PXI STAR Trigger (4)PXI Trigger Bus[5] (SSI) (5)SMB Trigger I/O *GA 3~8 could use (2), (4), (5) as output signal
Trigger Mode	Pre-Trigger, Post-Trigger, Middle-Trigger, Delay-Trigger
AFI (Auxiliary Function Interface)	
Number of Channel	8 input/output (refer to pin legend definition)
Compatibility	TTL / CMOS
Input Logic Levels	Input low voltage: 0.8V (max) Input high voltage: 2.0V(min)

Output Logic Levels	Output low voltage: 0.4V (max) Output high voltage: 2.8V (min)
Output Driving Capacity	±24mA
Maximum Input Overload	-0.5 V ~ +5.5 V
Trigger Condition	Rising or Falling, software selectable
Minimum Pulse Width	12.5 ns
Power-on State	Input, pull-low with 10KΩ resistor
Data Transfer	Polling mode
PXI STAR Trigger	
Receive Trigger from	PXI STAR Trigger
Compatibility	Input 3.3V or 5V TTL Output 3.3V TTL
Pulse Duration	12.5 ns
Pulse Logic	Rising or Falling edge, software selectable
PXI Trigger Bus[0..7]	
Receive Trigger from	PXI Trigger Bus line 5
Compatibility	Input 3.3V or 5V TTL Output 3.3V TTL
Pulse Duration	12.5 ns
Pulse Logic	Rising or Falling edge, software selectable

Digital I/O

Model Name	PXI-2022
Number of Channel	4 input/output
Compatibility	TTL / CMOS
Input Logic Levels	Input low voltage: 0.8V (max) Input high voltage: 2.0V(min)
Output Logic Levels	Output low voltage: 0.4V (max) Output high voltage: 2.8V (min)
Output Driving Capacity	±24mA
Power-on State	Input, pull-low with 10KΩ resistor
Data Transfer	Polling mode

General Purpose Timer/Counter (GPTC)

Model Name	PXI-2022
Number of Channels	2 up/down counter/timers (by AFI)
Resolution	32-bit
Compatibility	Input 3.3V or 5V TTL Output 3.3V TTL
Base clock available	20MHz
Data Transfer	Polling mode

Timebase System

Model Name	PXI-2022
Timebase Source	(1) Internal: onboard 80MHz oscillator (2) External from hardware IO
Sampling Rate Range	Timebase divided by 32-bit counter. TIMEBASE(80MHz) divider to the achieve equivalent sampling rate of DAQ. The equation is:

	Sampling rate = TIMEBASE / ScanIntrv The value of TIMEBASE depends on the card type. Take PXI-2022 (250KS/s) as an example, the ScanIntrv = 320 results in 250KS/s and ScanIntrv = 640 results in 125KS/s, and so on.
Internal Timebase Accuracy	<±25ppm (typical)
External Timebase Clock	
Sources (External from hardware IO)	(1) PXI_10M (2) AFI [0..7] (3) PXI Trigger BUS[0] (4) PXI Star Trigger
Dedicate External Clock Input From IO Connector	
Clock Type	Digital TTL
Input Frequency Range	1MHz ~ 20MHz
Input Coupling	DC
Input Compatibility	Input 3.3V or 5V TTL Output 3.3V TTL

Auto Calibration

Model Name	PXI-2022
Onboard reference	+5.000 V
Recommended warm-up time:	15 minutes
Temperature drift	±3 ppm/°C
Stability	50 ppm/1000hrs

General

Model Name	PXI-2022
Dimensions	Single 3U PXI module, 100mm by 160mm (not including connector)
Connector	ACL-10568-1, 68-pin VHDCI-type female
Operating Environment	Ambient temperature: 0 to 55°C Relative humidity: 10% to 90% non-condensing
Storage Environment	Ambient temperature: -20 to 80°C Relative humidity: 5% to 95% non-condensing

Power Requirements

Model Name	PXI-2022
+3.3V	1.5 A (typical)
+5V	1.3 A (typical)
+12V	0.35 A (typical)

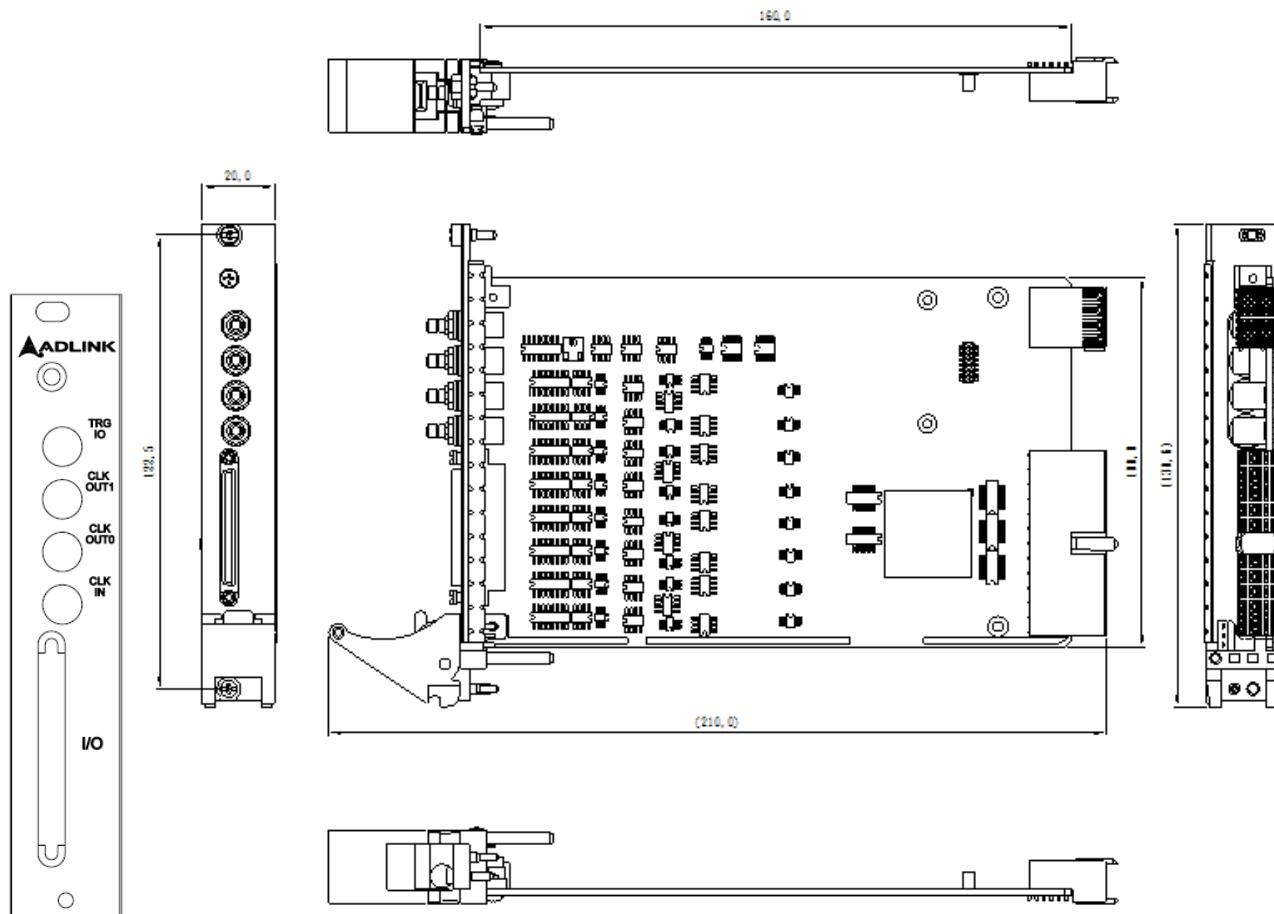
Pin Assignment : Connector Pin Assignment

	Pin #	Pin #	
DGND	34	68	DGND
DIO1	33	67	DIO0
DIO3	32	66	DIO2
DGND	31	65	AFI0/AD_TRIG_OUT
AFI1/AD_SAMPLE_CLK_OUT	30	64	AFI2/GPTC_CLK0
DGND	29	63	AFI3/GPTC_GATE0
AFI4/GPTC_CLK1	28	62	AFI5/GPTC_GATE1
AFI6/GPTC_Out1	27	61	AFI7/GPTC_Out0
NC	26	60	NC
NC	25	59	NC
AIL0	24	58	AIH0
AIL8	23	57	AIH8
AGND	22	56	AGND
AIL1	21	55	AIH1
AIL9	20	54	AIH9
AGND	19	53	AGND
AIL2	18	52	AIH2
AIL10	17	51	AIH10
AGND	16	50	AGND
AIL3	15	49	AIH3
AIL11	14	48	AIH11
AGND	13	47	AGND
AIL4	12	46	AIH4
AIL12	11	45	AIH12
AGND	10	44	AGND
AIL5	9	43	AIH5
AIL13	8	42	AIH13
AGND	7	41	AGND
AIL6	6	40	AIH6
AIL14	5	39	AIH14
AGND	4	38	AGND
AIL7	3	37	AIH7
AIL15	2	36	AIH15
AGND	1	35	AGND

Connector Signal Description

Pin #	Signal Name	Reference	Direction	Description
58, 55, 52, 49, 46, 43, 40, 37, 57, 54, 51, 48, 45, 42, 39, 36	AIH <0..15>	AIL <0..15>	Input	Differential positive input for AI channel <0..15>
29, 31, 34, 68,	DGND	-----	-----	Digital ground
24, 21, 18, 15, 13, 9, 6, 3, 23, 20, 17, 14, 11, 8, 5, 2	AIL <0..15>	-----	Input	Differential negative input for AIL channel <0..15>
1, 4, 7, 10, 13, 16, 19, 22, 35, 38, 41, 44, 47, 50, 53, 56	AGND	-----	-----	Analog ground for AI
65	AFI0	DGND	Input/Output	Auxiliary Function Input 0 (AD_TRIG_SRC0, AD_TIMER_SRC0, AD_CONV_SRC0)/AD TRIG Out

30	AFI1	DGND	Input/Output	Auxiliary Function Input 1 (AD_TRIG_SRC1, AD_TIMER_SRC1, AD_CONV_SRC1)/(AD SAMPLE CLK Out)
64	AFI2	DGND	Input	Auxiliary Function Input 2 (TRIG_SRC2, CLK_SRC2, GPTC_CLK0)
63	AFI3	DGND	Input	Auxiliary Function Input 3 (TRIG_SRC3, CLK_SRC3, GPTC_GATE0)
28	AFI4	DGND	Input	Auxiliary Function Input 4 (TRIG_SRC4, CLK_SRC4, GPTC_CLK1)
62	AFI5	DGND	Input	Auxiliary Function Input 5 (TRIG_SRC5, CLK_SRC5, GPTC_GATE1)
27	AFI6	DGND	Input/Output	Auxiliary Function Input 6 (TRIG_SRC6, CLK_SRC6)/(GPTC_OUT1)
61	AFI7	DGND	Input/Output	Auxiliary Function Input 7 (TRIG_SRC7, CLK_SRC7)/(GPTC_OUT0)
67, 33, 66, 32	DIO<0..3>	DGND	Input/Output	Programmable DIO pins for Polling mode
25, 26, 59, 60	NC	DGND	-----	-----



The ADLINK PXI-2022 is packaged in a Euro-card form factor compliant with PXI specifications measuring 160 mm in length and 100 mm in height (not including connectors). The connector types and functions are described as follows.

SMB Connector

- SMB Connector 1 : TRG IO

- SMB Connector 2 : Sync CLK_OUT1 (for multi-chassis synchronization)
- SMB Connector 3 : Sync CLK_OUT0 (for multi-chassis synchronization)
- SMB Connector 4 : CLK IN (for multi-chassis synchronization)

Connector	Direction	Type	Description/Function
TRG IO	Input Output	SMB	The TRG IO is a bidirectional port for external digital trigger input or output.
CLK OUT1	Output	SMB	The CLK OUTOUT 1 is a 50Ω, DC-coupled output; CLK_OUT0 and CLK_OUT1 is from the same source.
CLK OUT0	Output	SMB	The CLK OUTPUT 0 is a 50Ω, DC-coupled output; CLK_OUT0 and CLK_OUT1 is from the same source.
CLK IN	Input	SMB	The CLK IN is a 50Ω, AC-coupled external timebase input.

TRG IO, as input port	
Connector type	SMB
Compatibility	3.3 V LVTTTL(Low Voltage), 5 V tolerant
Input Logic Level	Input Low voltage:0.8V (max) Input high coltage:2.0 (min)
Maximum Input Overload	-0.5 V to +5.5 V
Trigger Polarity	Rising edge or falling edge (Software programmable)
Minimum Pulse Width	12.5 ns

TRG IO, as output port	
Connector type	SMB
Compatibility	3.3 V TTL
Output Logic Level	Output low voltage: 0.2V (max) Output high voltage: 2.4V (min)
Driving Capability	8 mA
Minimum Output Pulse Width	12.5 ns

CLK IN (external clock from front panel)	
Connector Type	SMB
Clock Type	Sine wave or square wave
Input Impedance	50 Ω
Input Coupling	AC
Input Range	1 VP-P to 2 VP-P
Overvoltage Protection	2.5 VP-P

CLK OUT0/OUT1, as output port	
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Connector Type	SMB
Clock Type	square wave
Compatibility	3.3 V TTL
Output Logic Level	Output low voltage: 0.2V (max) Output high voltage: 2.4V (min)
Driving Capability	8 mA
Output Impedance	50 Ω

Accessories

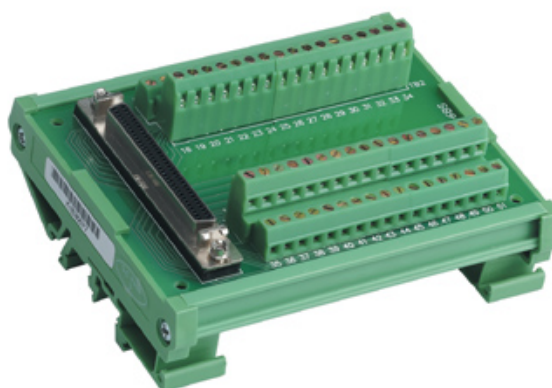
- **SMB-SMB-1M**
1 meter SMB to SMB cable
- **SMB-BNC-1M**
1 meter SMB to BNC cable

Terminal Boards

- **DIN-68S-01**
Terminal Board with One 68-pin SCSI-II Connector and DIN-Rail Mounting (cables are not included; for information on mating cables, refer to Section 12, Accessories.)



Termination board DIN-68S-01 &
68-Pin SCSI-VHDCI cable ACL-10568-1



Cable

- **ACL-10568-1**
68-pin SCSI-VHDCI cable, 1m

Ordering Information

- PXI-2022 :
 - 16-bit, 250KS/s, 16 Channels Simultaneous Sampling Card